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Device and array for a 10^7 bit high density magnetic thin film memory

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Device and array for a 10^7 bit high density magnetic thin film memory

by

Dan Karmon

A Dissertation Submitted to the
Graduate Faculty in Partial Fulfillment of
The Requirements for the Degree of
DOCTOR OF PHILOSOPHY

Major Subject: Electrical Engineering

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I. INTRODUCTION

Magnetic planar thin film memories have been built and proposed for three typical levels of memory hierarchies: the scratch-pad, main memory, and bulk storage. Rapid development in integrated circuit technology has resulted in the dominance of scratch-pads by various integrated circuit memory devices. Despite predictions, great commitment and marketing efforts, the magnetic core is still dominating the main storage devices. However, the magnetic film memories should and can have their impact on main memories. Work on large thin film memories is not new (1, 2). Several memories have been produced both in the main and bulk categories (3, 4, 5, 6, 7).

The development of any random access memory technology for main and bulk memory application is aimed at:

a) high data rates

b) large capacity

c) lower power

and most important

d) low cost

The highest operating speeds of magnetic storage devices are realized with planar magnetic films. Coupled with batch fabrication of film elements, this type of memory offers the best possible performance/cost ratio.

Magnetic planar film memories have been used in the destructive and nondestructive readout modes. DRO historically found limited application as scratch-pad devices and are usually slower, and in the past, cost more

than the NDRO memory. However, with changing design objectives due to technical and concept development, DRO devices should be given a second look.

The design objectives of high data rates and low cost imply a long word, minimum connections, and high density devices. Keeping such objectives in mind a case can be made for the DRO memory. Such a memory can be built (as will be shown) with the following characteristics. A semi-closed hard direction device using coupled films and continuous mechanically defined strips in the easy direction. The device is an integral word-line structure of sputtered Permalloy film and copper which forms 2 mil wide word lines on 4 mil centers, 8-10 inches long. The sense-digit lines are made of multiturn windings of 3 turns on 12 mil centers and are 16.5 inches long. Such a memory module, using two back to back substrates will have at least 830 bits per word and 8000 word lines per digit line (or 4000 lines per digit line for two magnetic spots per bit). The long words are required for high data rates, and the high density of word lines is essential for keeping electronics cost down and reducing the number of connections. This memory will have a word current of 100mA, digit current of 12mA, and a cycle time of about 500 nsec. It is important to note that a 5:1 increase in memory system speed can be realized when such a memory is used in conjunction with the Cache memory concept.

A NDRO memory of a similar structure can be built (8). Upon close examination it turns out that such a device will favor the semi-closed easy axis structure. The device is an intergral sense-line structure of evaporated Permalloy films and copper. The design limits the copper

sense-digit lines to 5 mil width on 8 mil centers. The 3 turn word lines are on 10 mil centers. The basic modules is limited to 3160 word lines and 316 sense digit lines.

A lower data rate is an obvious characteristic of such a device. It should be noted that due to the lower density ten modules are required (versus 4 for the DRO memory) for a 10^7 bit device. The cost of connections will contribute heavily to the cost increase in such a memory. Further examination reveals the electronics cost to be about equal.

It is the intent of this study to show that high density DRO memory arrays can be fabricated with special purpose, simple and functional integrated circuits. With special attention to connections, cost can be kept low. Various line densities and array configurations are tested for a partially populated memory. The performance of a fully populated memory is predicted.

II. LITERATURE REVIEW

Since 1955 the physics, behavior and fabrication of magnetic thin films have been studied extensively.

Most of the early work on thin-film memories has been reviewed by Pohm and Mitchell (9). In the beginning numerous problems have plagued thin film elements, including dispersion, magnetostriction, and yield. Since acceptable films are now made in a routine fashion by vacuum deposition (widely reported), sputtering (10), and electroplating (11), there has been a concentrated effort and interest in reaching other goals. Lower cost, higher bit density, lower drive currents, and faster cycle time became primary interests in the development of new film memories.

Raffel, Crowther, and Chang (12, 13, 14) are among the many who investigated the use of coupled closed flux film elements which contributed to the further development of higher density and lower drive memories. A good review of the design objectives and considerations was presented by Pohm and co-authors in 1963 and 1968 (15, 16).

A large "manufacturable 120 nsec cycle magnetic film memory containing 600,000 bits in the basic module" was reported by Pugh, Shahan, and Siegle (17). This memory, like all others reported devices, has low density and high drive currents (although, compatible with core memories). The above mentioned memory had a 25 x 30 mil bit size with a corresponding density of about 620 bits per inch^2. The drive currents were 510mA for the read cycle and 100mA digit current. In 1968 Raffel and co-authors (18) reported on a large capacity memory. Crowther (19) presented the

specifications and parameters for a design of such a memory. This device featured a density of 12,500 bits/in^2 and its read and digit current were 500mA and 160mA respectively.

During this period of concentrated effort of building large memories, other more specific problems were investigated. The problems of metallic underlayers (20), vacuum deposition processes (21), dispersion creep and switching speed (22), and copper diffusion problems (23) were investigated. Studies such as these have contributed to the steady improvements of planar magnetic thin film memories. Batch fabrication, multilayer integrated films and performance characteristics improved steadily. Despite the fact the current interest does not lie with planar thin film memories, several important reports (4, 5, 24) indicate that it is possible to manufacture economically, large main memories using magnetic thin films.

Raffel and co-authors (4) reported a study of a 10^7 bit memory of 900 nsec cycle time. This DRO memory uses long digit lines (50 inches) to reduce cost and 336 bits per word for high data rates. Using high H_c and H_k coupled films, the reported word and digit currents are 400mA and 225mA respectively. The General Electric report (5) describes a 3500 bits/in^2 memory. With specially developed monolithic drive and sense circuits, the cost estimate for a 128 Kbyte (72 bits per word organization) is 0.5 ¢/bit. The memory has a 200 nsec cycle time and 70 nsec access time. Word and digit currents are 200-250mA and 70mA respectively. Special attention to integration resulted in 40,000 bits per substrate.

Pohm and co-authors (24) reported on a DRO planar magnetic film memory cell. Using low H_c and H_k coupled hard direction structure this array has the potential to have densities of up to 64,000 bits/in^2. A 16,000 bit/in^2 partially populated array required 100mA word current and 8-12mA of digit current with 5-7mv output signals.

This device is the subject of investigation presented in this thesis. By further development and experimental work it will be shown that a memory with higher density, lower drive current and cost can be built.

III. BASIC DESIGN CONSIDERATIONS

A. Introduction

It has been shown (24) that very effective, high density, DRO magnetic film memory arrays can be constructed which are compatible with integrated circuit currents, power levels and packaging.

The array to be constructed is a high speed, large capacity one. Such characteristics require high bit densities and improved techniques to minimize undesirable coupling between drive and sense lines. Pohm and co-workers (24) have demonstrated that high density, and good performance are possible with existing fabrication techniques.

Using (24) as a point of departure some features of the array are taken as proven ones. The general structure and materials used are the same. The object of this chapter is to investigate the magnetic film constants, consider the size and organization of the full array, and investigate the effect of physical properties in light of the general objective of this work.

The structure to be presented later is characterized by high density and low drive currents. In order to obtain a high density memory one needs to reduce drive line width. In the structure under study the word line width is 2 mils. The width of the line needs to be reduced for other purposes too. The magnetic field per unit drive current is proportional to 1/line width (and thus film width). The film output signal is proportional to the magnetic flux, film thickness and width. In order to reduce word drive current, and at the same time, maintain

signal level, the width of the word line has to be decreased, and the film thickness increased. Note, however, that since the demagnetizing field is proportional to the film thickness squared, an element might not stay in a single domain state.

In order to reduce or eliminate the demagnetizing field the following methods are employed:

Keepering for partial close flux path which can result in a 70% demagnetizing field cancellation (25).

A coupled device which gives a semi-closed path. This is done by using an identical film pair. The structure chosen is a Closed-Hard-Axis device. Such a device is closed during reading which reduces the word current. This structure also gives high output signal (as compared with Closed-Easy-Axis devices), and low word line to word line interaction all serving the high density objective. The main disadvantage of such a device is the increased demagnetizing field along the easy-axis which reduces the density of the digit lines. The ferrite keeper material will partially cancel this effect.

B. Element Structure and Specifications

In order to reduce interaction noise (26) due to ground current spreading, the ground plane should be chosen to be as thin as possible. A further improvement can be obtained if about 20,000 Å Permalloy are deposited on the ground plane. The structure of the memory element is shown in Figure 1.

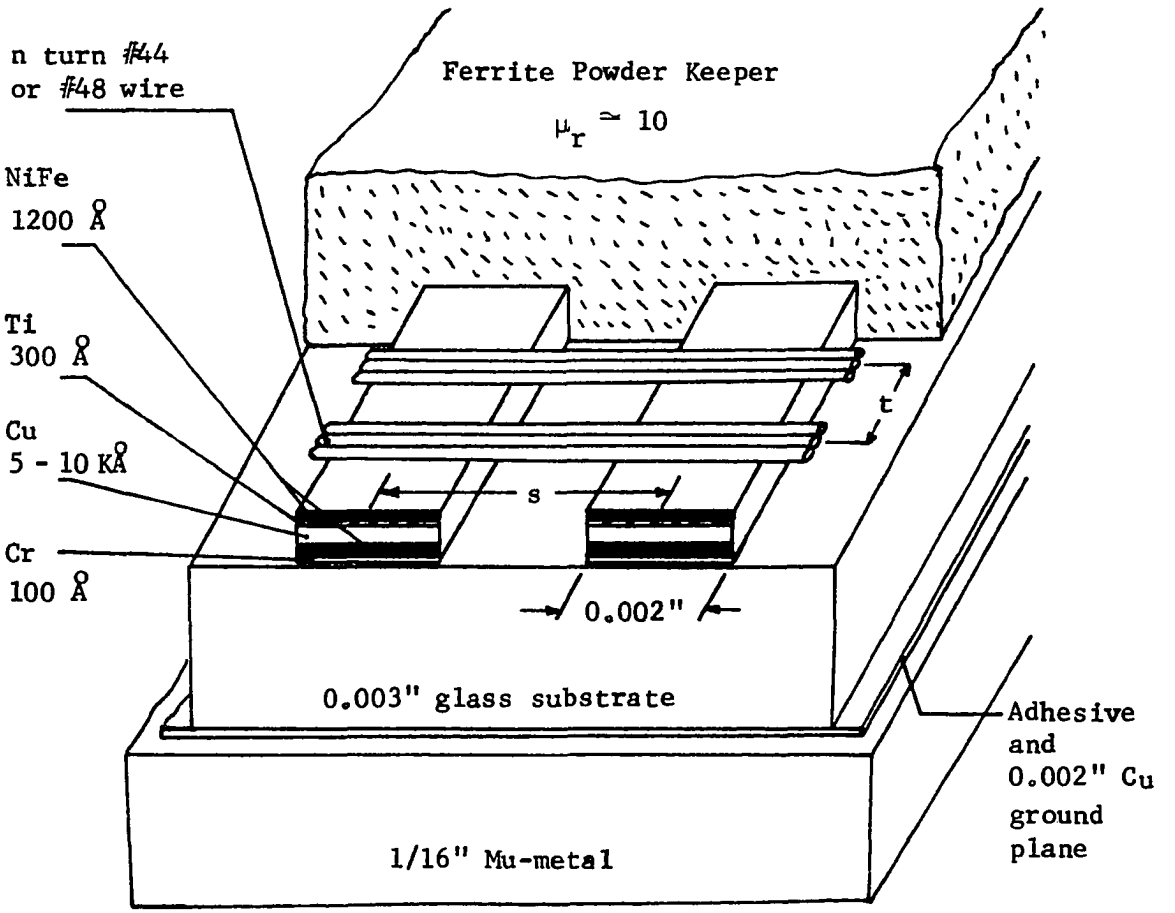


Figure 1. Element geometry

The parameters t, s, and the word line thickness (copper line) are determined later. Also to be determined is the number of turns n, and the wire to be used for the sense line.

In general, for an open flux structure, demagnetization fields and drive currents limitations dictate some maximum anisotropy field H_k and minimum coercive force H_c. Assuming 1200 Å thick Permalloy films,

one can calculate these fields (27).

Assume the following:

Saturation magnetization of 10,000 gauss, word line width 2 mils, α_{90} is assumed to be 0.085 H_c/H_k; the demagnetizing field in the hard direction is reduced by a factor of about 4 due to the closed structure. Word currents to be considered are 80, 100, 120mA. In the easy direction the demagnetizing field is considered as for a 2400 Å single film, the demagnetizing field in the easy direction will be reduced by a factor of about 3 due to effective keepering.

In an open flux structure, the maximum tolerable anisotropy $H_{k(max)}$ is dictated by the word current and the demagnetizing field in the hard direction. A net field of $H_{k(max)}$ is required to rotate the magnetization.

$$H_{k(max)} = \frac{I_w}{4w} - H_{dh} \; ; \quad H_{dh} = 1.5 \frac{B_s t}{w}$$

where: H_{dh} = demagnetizing field in the hard direction

w = word line width

B_s = saturation magnetization

t = film thickness

The minimum wall coercive force $H_{c(min)}$ is defined as

$$H_{c(min)} = (\rho+1)H_{de} + \rho H_k \alpha_{90}$$

$$\rho \equiv \frac{H_c - H_{de}}{H_{de} + H_k \alpha_{90}}$$

$$H_{de} = \frac{B_s t}{L}$$

where: H_{de} = easy axis demagnetization

L = effective digit width

Substituting the assumed α_{90}

$$H_{c(min)} = \frac{(\rho+1)\, H_{de}}{(1 - 0.085\rho)}$$

The results for $H_{k(max)}$ and $H_{c(min)}$ as a function of sense and word line width are depicted in Figure 2.

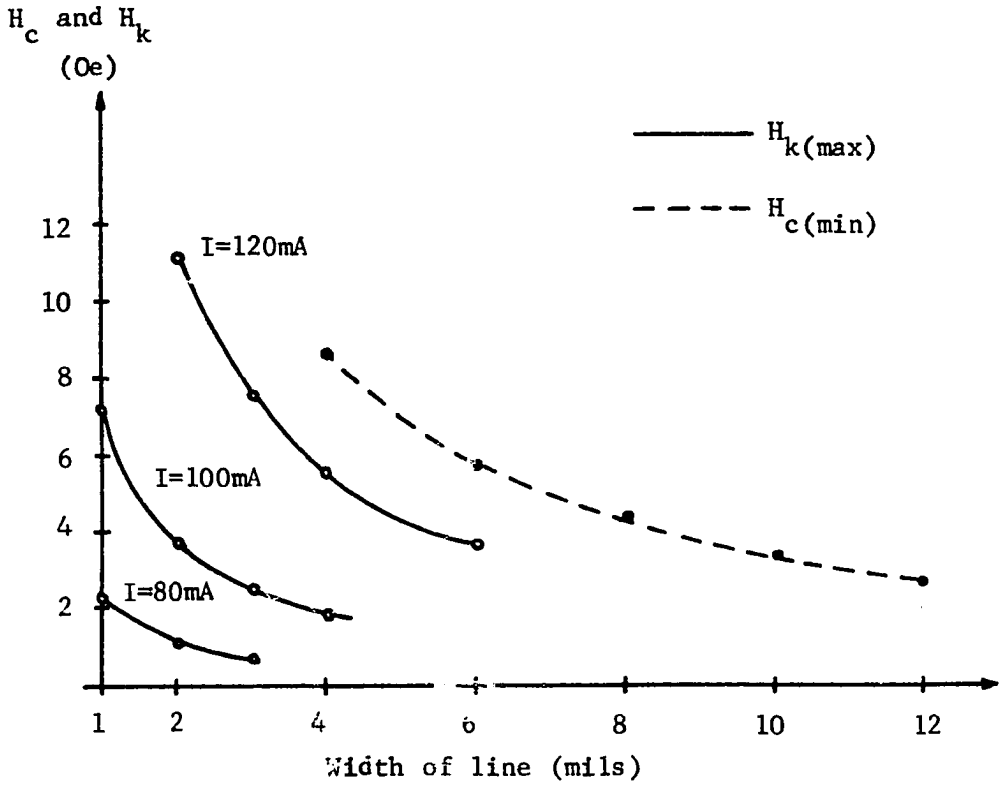


Figure 2. Required $H_{k(max)}$ and $H_{c(min)}$ vs. line width

From Figure 2 it seems that the following specifications should be met:

$H_{k(max)} = 5$ Oe $W = 2$ mil $I_w \tilde{=} 110$mA

$L = 12$ mil $H_{c(min)} = 3$ Oe $\rho = 1^+$

These results are compatible with the array described by Pohm and co-workers (24). The effective width L of 12 mils is analogous to 5 turns of #48 (1.6 mil od.) wire, and α_{90} assumed is analogous to an easy axis skew of about 3^o.

C. Capacitance of Word and Sense Line

The distributed capacitance of a memory element is approximated by the parallel plate capacitance formula (MKS units).

$$C(pF) = \frac{8.80 \times \text{Area} \times \text{Relative dielectric constant}}{\text{Thickness of insulation}}$$

The calculations below are for capacitance per mil (width of the sense line), and for wire #48 only.

$$C_w \equiv \text{Word line to ground} = \frac{8.8 \times 2 \times 4}{3} \times 2.5h \times 10^{-5}$$
$$= 59.5 \times 10^{-5} \text{ Pf/mil}$$

$$C_d \equiv \text{Digit line to ground}$$
$$= \frac{8.8 \times 2 \times 3}{0.4 + 0.1} \times 2.54 \times 10^{-5} + \frac{8.8 \times 2 \times 4}{3 + 0.1} \times 2.54 \times 10^{-5}$$
$$= 326 \times 10^{-5} \text{ Pf/mil}$$

C_{wd} = Word line to digit line

$$= \frac{8.8 \times 2 \times 4}{2 + 0.4 + 0.1} \times 2.5h \times 10^{-5} + \frac{8.8 \times 2 \times 3}{0.1} \times 2.54 \times 10^{-5}$$

$$= 1371.5 \times 10^{-5} \text{ pF/mil}$$

$\therefore$ The capacitance/mil for sense and word line is

$C_t \simeq 0.0176$ pF/mil

D. Word and Sense Line Characteristics

1. Word line

a. Resistance The word line is a copper strip 2 mils wide. Thicknesses to be considered are 5000 Å to 20,000 Å. The return path for the drive current is the ground plane; the line is shorted at its far end. Some approximations of the line characteristics follow.

Due to the skin-effect, resistance increases as the operating frequency goes up. For conductors with a thickness much greater than the depth of penetration δ, the skin-effect is:

$$R_s = \frac{1}{w \delta \sigma} \ \Omega \text{ per unit length for } \quad \delta = \sqrt{\frac{2}{\omega \mu \sigma}}$$

w = width

σ = conductivity

Usually, the thickness of the conductor is comparable, or less than the penetration depth. The modified formula for the skin-effect resistance is:

$$K_s = \frac{1}{w \sigma \delta} \quad \frac{\sinh \frac{2B}{\delta} + \sin \frac{2B}{\delta}}{\cosh \frac{2B}{\delta} - \cos \frac{2B}{\delta}} \qquad \Omega \text{ per unit length}$$

$$= \frac{1}{w \sigma \delta} K$$

The resistance for a line w wide and B thick is then given by $R = R_{DC}(1 + \eta)$ per unit length (28), where: $\eta = \frac{BK - \delta}{\delta}$

For the memory under consideration (cycle time ≥ 200 nsec) the ratio $B/\delta \leq .01$. For this ratio $\eta \ll 10^{-4}$ (28) and the R_{DC} approximation will be used. The resistance calculations assume the resistivity of copper to be 2×10^{-6} Ω cm. The results are depicted in Figure 3.

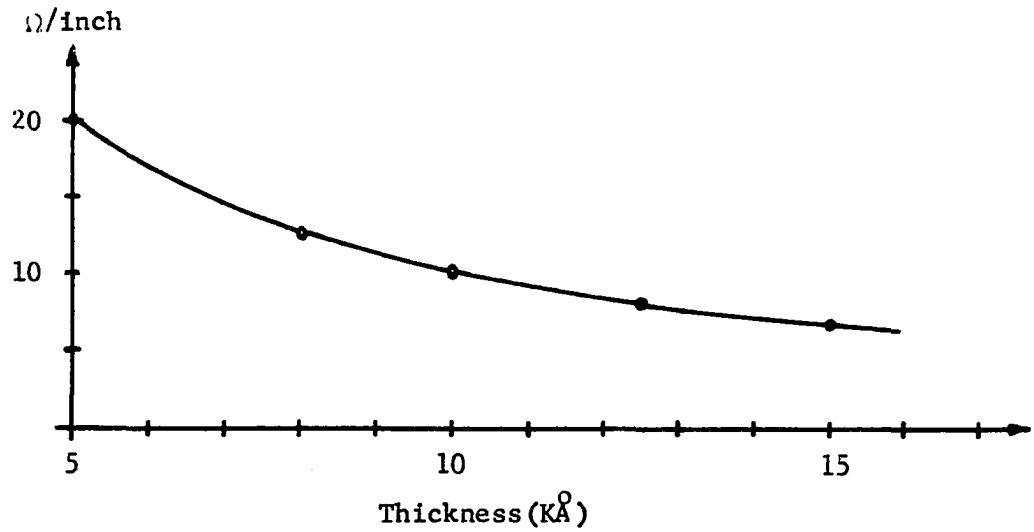
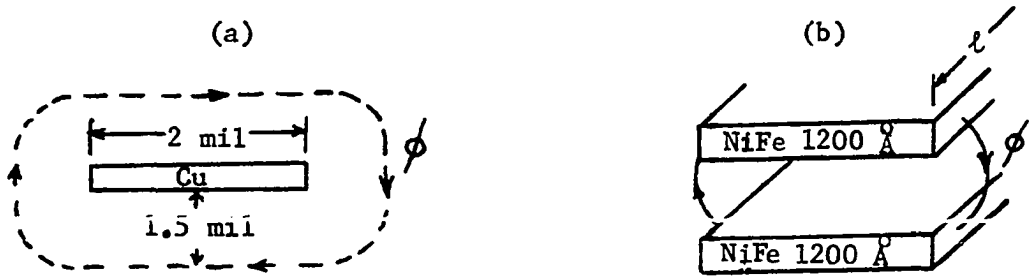


Figure 3. Word line resistance vs. thickness

b. Inductance Assuming the geometry shown below, the inductance of the word line can be calculated. Two components need to be considered a) air gap inductance, b) the magnetic material loading.



a) air gap

$$H = \frac{1.26\ I}{2w} = \frac{1.26\ I}{2 \times 5 \times 10^{-3} \times 2.54} \simeq 49\ \text{Oe/A}$$

$$B = \mu_o H = 4\pi \times 10^{-7} \times 49 \times \frac{10^3}{4\pi} = 49 \times 10^{-4}\ \text{Wb/m}^2\text{A}$$

$$\text{L/unit length} = 49 \times 10^{-4} \times 3 \times 10^{-3} \times 2.54 \times 10^{-2} \simeq 0.38\ \mu\text{H/m}$$

$$\simeq 0.96 \times 10^{-11}\ \text{H/mil}$$

b) for $B_s = 10^4$ Gauss

$$\phi\text{/unit length} = 1 \times 1200 \times 10^{-10} = 0.12 \times 10^{-6}\ \text{Wb/m}$$

The inductance per meter vs. word current I_w is depicted in Figure 4.

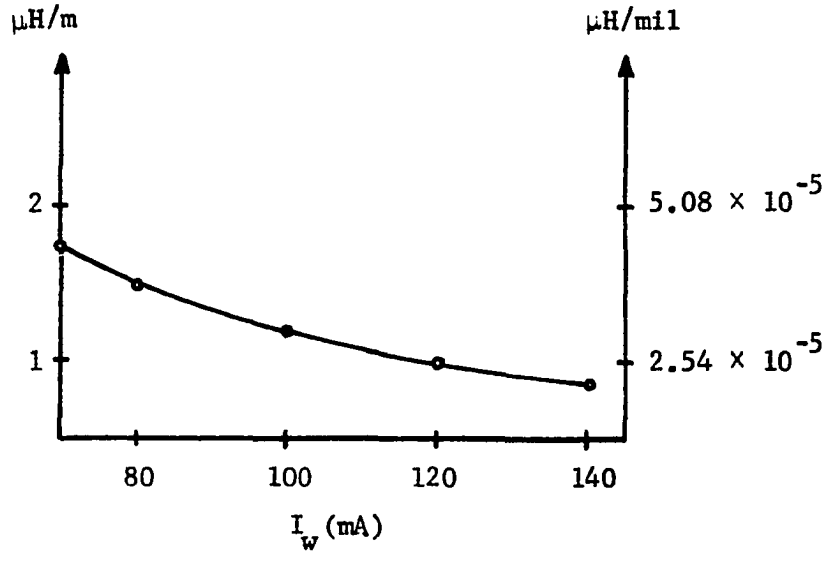


Figure 4. Magnetic material inductance along the word line

c. Element delay and characteristic impedance As the drive current has a short rise time corresponding to high frequency component a small-loss approximation will be made (28, 29). The distortionless approximation will also be used; this might require additional resistive loading.

$$\tau/\text{element} = \sqrt{LC} =$$

$$\{(9.6 \times 10^{-12} \times \text{effective width of sense line} + 30.5 \times 10^{-12} \times \text{effective width of sense line})$$

$$\times (0.0176 \times 10^{-12} \times \text{width of sense line})\}^{\frac{1}{2}}$$

Assuming for the above: 100mA word current, an effective sense line width 4 mils wider than the actual width, #48 wire, and inductance including the magnetic loading (Figure 4).

The characteristic impedance Z_o is given by $Z_o = \sqrt{L/C}$

$$Z_o = \{(\text{effective width of sense line} \times 40.1 \times 10^{-12})/$$

$$(0.0176 \times 10^{-12} \times \text{width of sense line})\}^{\frac{1}{2}}$$

Table 1 shows the results obtained.

Table 1. Time delay per element and characteristic impedance of a multiturn sense line

# of sense line turns	2	3	4	5
τ/element (nsec)	.004	.0055	.0068	.0082

# of sense line turns	2	3	4	5
$Z_o(\Omega)$	72	65	61	59

d. Delay and attenuation The down and back delay can be calculated from the per element delay. The down and back attenuation can be calculated from the known resistance and characteristic impedance. Most calculations are done for a 5 turn sense line. Word line thicknesses 5000 Å and 10,000 Å are considered with resistance 20Ω/inch and 10Ω/inch respectively. Line lengths under consideration are from 2 to 10 inches. Various element densities are also examined.

The down and back delay $\equiv \tau_{dB}$

$= (\tau$ per element $\times$ # elements/inch $\times$ length) $\times$ 2

The down and back attenuation $\equiv A_{db}$

$= e^{-2(R/\text{inch} \times \text{length})/2Z_o}$

given: R/inch = 20Ω/inch , 10Ω/inch

$Z_o \simeq 60\Omega$ (For 5 turn sense line)

τ/element = 0.0082 nsec/element (p.10)

Density of sense lines $\equiv D_s$ = 125,80,60,50 element/inch

The tables (2, 3, 4) below show the results. Also shown is the RC approximation for 10,000 Å thick line with C = 0.0176 pF/element. Figure 5 shows the results graphically.

Table 2. Down and back attenuation (A_{db}) of the word line

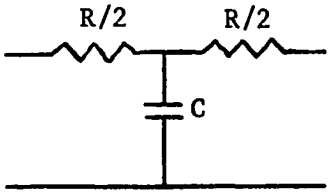
Length of line (inch)	2	4	6	8	10
20Ω/inch line, 5 turn sense line	.50	.25	.128	.065	.033
10Ω/inch line, 5 turn sense line	.71	.50	.36	.25	.18
10Ω/inch line, 3 turn sense line	.73	.54	.4	.28	.21

Table 3. Down and back time delay (τ_{db}) of the word line

	Length (inch)	2	4	6	8	10
D_s	125 elem./inch	4.1	8.2	12.3	16.4	20.3
	80 elem./inch	2.6	5.25	7.9	10.5	13.2
	60 elem./inch	1.97	3.9	5.9	7.9	9.88
	50 elem./inch	1.64	3.3	4.9	6.5	8.2

Table 4. RC approximation for the time delay of the word line

Length (inch)	2	4	6	8	10
RC (nsec)	1.76	3.5	5.3	7.0	8.8



R = 10Ω/inch

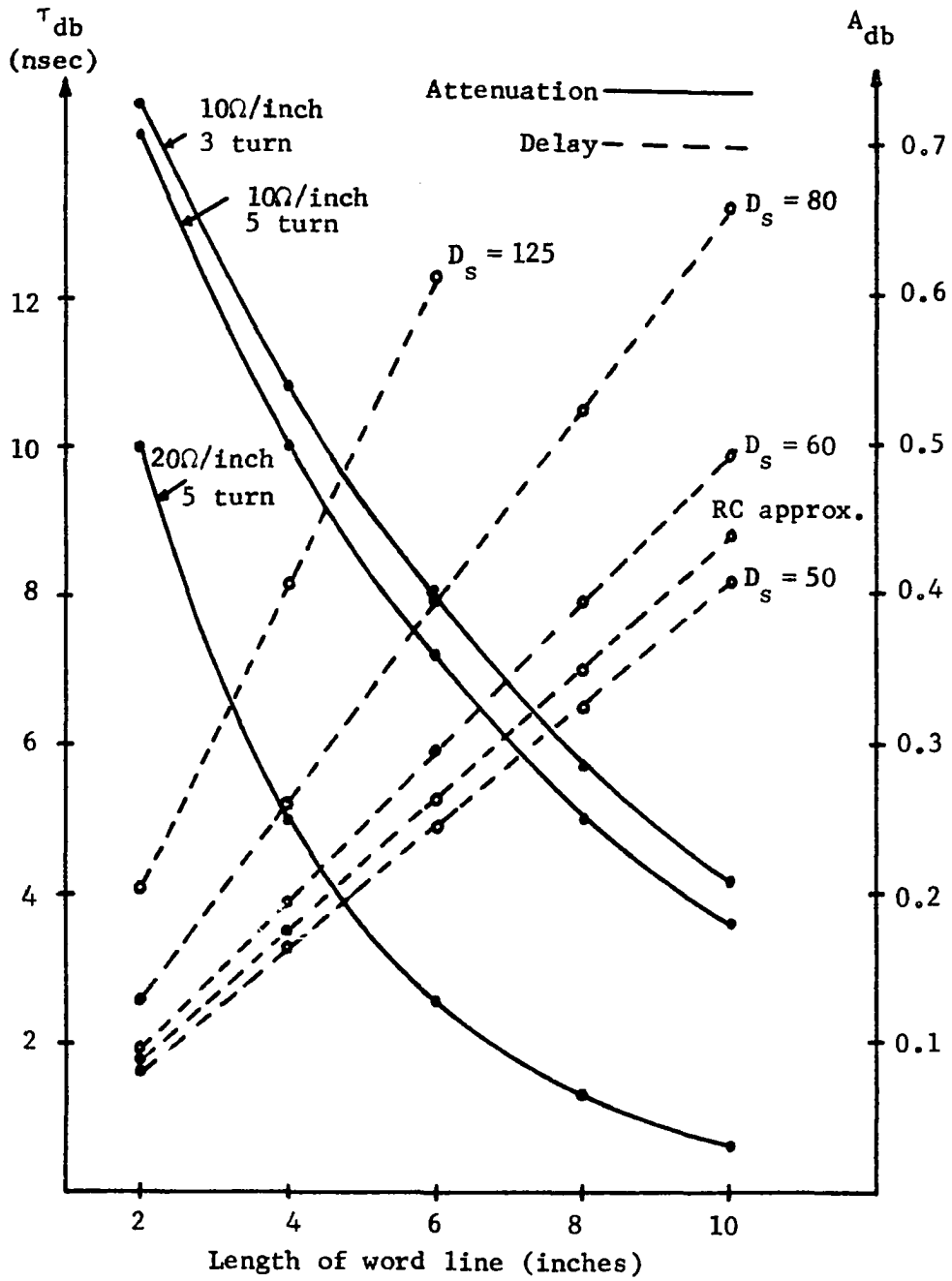


Figure 5. Down and back delay (τ_{db}), down and back attenuation (A_{db}), and RC approximation vs. word line length

2. Sense line

Since the word lines are very narrow, it is possible to use multiturn sense-digit lines. Although these will not be as dense as the word lines, it is still possible to link a significant number of elements.

The multiturn sense line depicted in Figure 1 can be approximated by the lumped parameter circuit shown below in Figure 6.

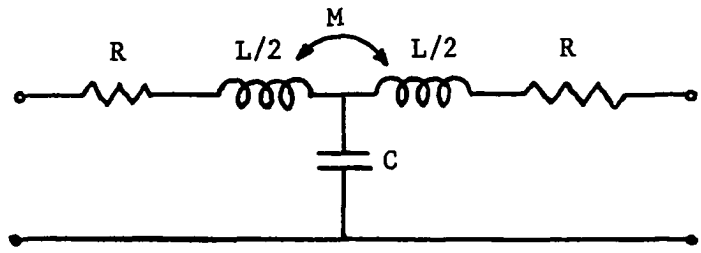


Figure 6. Lumped parameter approximation of the multiturn sense line

The maximum mutual inductance would be $\frac{L}{2}$. This type of transmission line is difficult to evaluate. An attempt will be made here to approximate this line in the same way the word line was handled. Experimental results will reveal the degree of inaccuracy.

a. Resistance For the sense-digit line two wires are under consideration, #48 wire - 0.0016 inches outer diameter, 0.0014 inches inner diameter and #44 wire - 0.0023 inches outer diameter, 0.0020 inner diameter (typical values).

Skin effect and additional reactance are ignored. The resistance modifications are $0.0003 < R < 0.008$ (Handbook of Chemistry and Physics, 43rd edition).

Figure 7 gives the resistance as a function of turns and length of the sense line. The #48 and #44 wires have a resistance of 6Ω/ft and 3.4Ω/ft respectively.

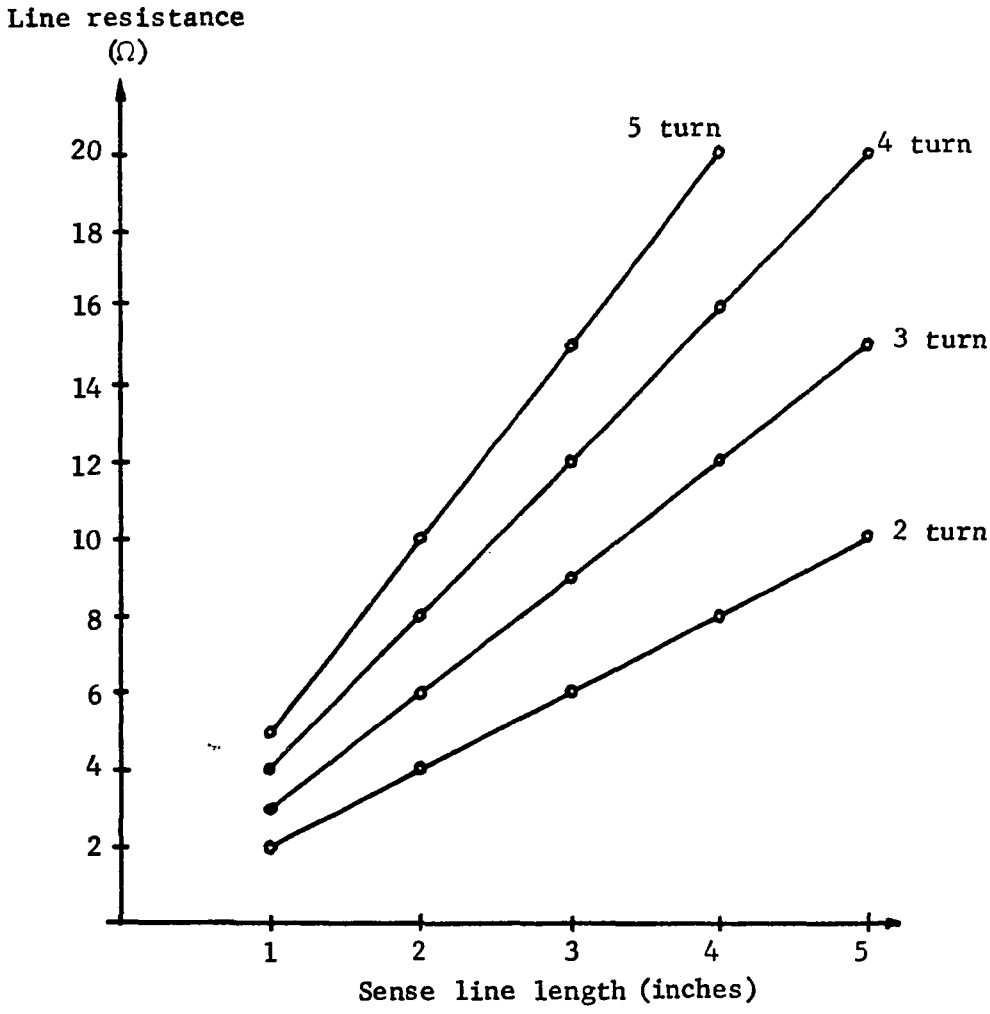


Figure 7. Sense line resistance

b. Inductance The inductance of the multiturn line is approximated by calculating the field contribution from all lines at point P as shown below. The image of the line current is included. The calculations are done for the two wires mentioned before and for word line thicknesses of 5000 Å and 10,000 Å. Figure 8 shows the geometry considered. Thicknesses of the element layers are as shown in Figure 1.

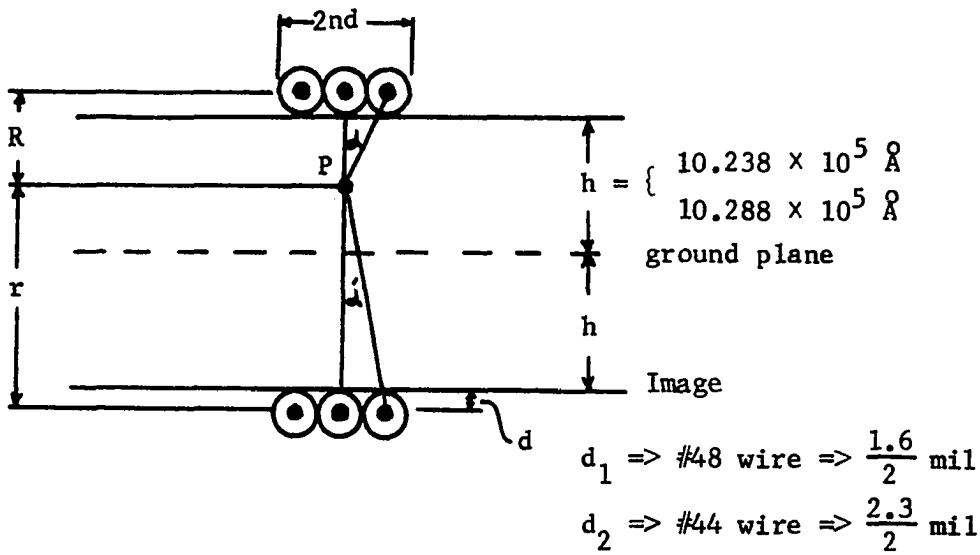


Figure 8. Multiturn sense line geometry

$$R_{(\#48)} = h/2 + d_1 \quad , \quad R_{(\#44)} = h/2 + d_2$$

$$r_{(\#48)} = h + d_1 + h/2 \quad , \quad r_{(\#44)} = h + d_2 + h/2$$

There will be very small inductance loading of the magnetic material along the digit line because the fields are applied in the remanent direction of the magnetic materials. Therefore, only the air gap inductance will be calculated.

The following equations describe the calculations made.

$$B = \mu_o \frac{I}{2\pi S}$$

$$B = \frac{2 \times 10^{-7}}{S} \cos\alpha \quad Wb/m^2A \qquad S^2 = (nd)^2 + R^2$$

$$L = B \times h \times n \qquad n = \text{number of turns}$$

The results are shown in Table 5 below and Figure 8. Note that in Figure 9 where 3 digit approximations are plotted the differences attributed to word line thickness are not discernible. The results shown are per mil length of the sense line.

Table 5. Inductance of sense line Henry/mil $\times 10^{-12}$

	# turns	2	3	4	5
5000 Å Cu	#48 wire	38.721	80.792	131.55	190.93
	#44 wire	33.956	68.834	110.07	155.71
10,000 Å Cu	#48 wire	38.780	80.947	131.95	191.41
	#44 wire	34.024	68.998	110.37	156.17

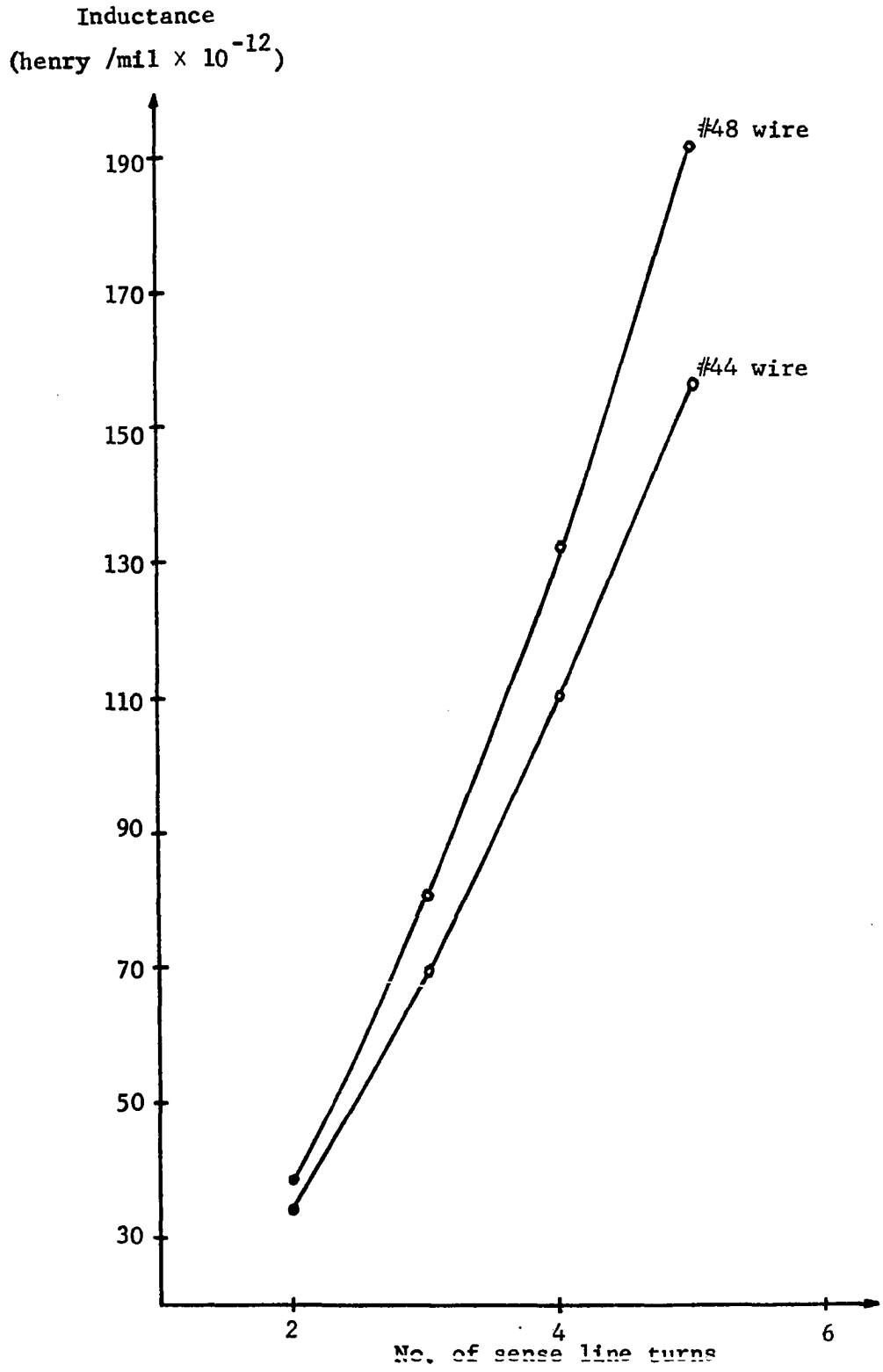


Figure 9. Inductance of the sense line vs. # of turns

c. Characteristic impedance Using the same procedure as before, Z_o will be calculated for #48 wire and word line densities D_w of 125 and 250 per inch.

$$Z_o = \sqrt{L/C} = \{(L/\text{mil} \times 10^{-12} \times \text{length})/ (0.0176 \times N^{-12} \times \text{width of sense line} \times D_w \times \text{length})\}^{\frac{1}{2}}$$

$$= \{ L/\text{mil} \times 10^{3}/0.0176 \times 2\text{nd} \times D_w \}^{\frac{1}{2}}$$

where: n is the number of turns

d is the radius of the wire (mils)

L/mil is from Figure 7 times 10^{12}

The results are shown in Table 6.

Table 6. Characteristic impedance of the sense line $Z_o(\Omega)$

# of turns		2	3	4	5
D_w	125 elem./inch	73	87	98	104
	250 elem./inch	52	62	69.5	73.5

d. Delay and attenuation The delay and attenuation for the sense line are calculated for different number of line turns n, word line densities D_w and line length ℓ. All calculations are for #48 wire.

One way delay $\equiv \tau_d = \sqrt{LC}$

$$= 10^{-3} \times \ell \times (28.16 \times n \times D_w \times L)^{\frac{1}{2}}$$

τ_d - nsec, D_w - 125, 250 elem./inch, ℓ - inches,

L - inductance per mil (Figure 7 $\times 10^{12}$)

Down and back attenuation $\equiv A_{db} = \ell^{-2(R/\text{inch} \times \text{length}/2 Z_o)}$

Tables 7, 8, and 9 show the results, also shown are the results for the L/R approximations which give a clue to the experimental results expected for the sense line approximations made. Figure 10 gives some of the plots of these results.

Table 7. One way delay τ_d(nsec)

Length of line (inch)			1	2	3	4	5
D_w = 125	# of turns	2	0.52	1.04	1.57	2.09	2.6
		3	0.92	1.83	2.77	3.68	4.62
		4	1.38	2.76	4.15	5.55	1.93
		5	1.83	3.66	5.5	7.34	9.13
D_w = 250	# of turns	2	0.74	1.48	2.2	2.96	3.74
		3	1.3	2.63	3.92	5.23	6.53
		4	1.96	3.92	5.88	7.75	9.8
		5	2.59	5.02	7.78	10.4	12.9

Table 8. L/R approximation

# of turns	2	3	4	5
τ (nsec)	9.7	13.5	17	19.2

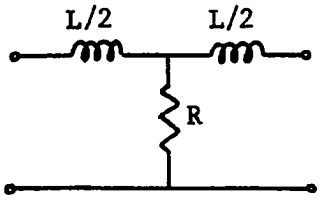


Table 9. Down and back attenuation A_{db}

Length of line (inch)			1	2	3	4	5
D_w = 125	# of turns	2	0.972	0.946	0.921	0.896	0.871
		3	0.966	0.933	0.901	0.871	0.891
		4	0.960	0.922	0.885	0.850	0.815
		5	0.953	0.908	0.865	0.825	0.786
D_w = 250	# of turns	2	0.962	0.925	0.891	0.857	0.825
		3	0.952	0.907	0.864	0.824	0.785
		4	0.944	0.891	0.841	0.794	0.750
		5	0.934	0.872	0.815	0.761	0.711

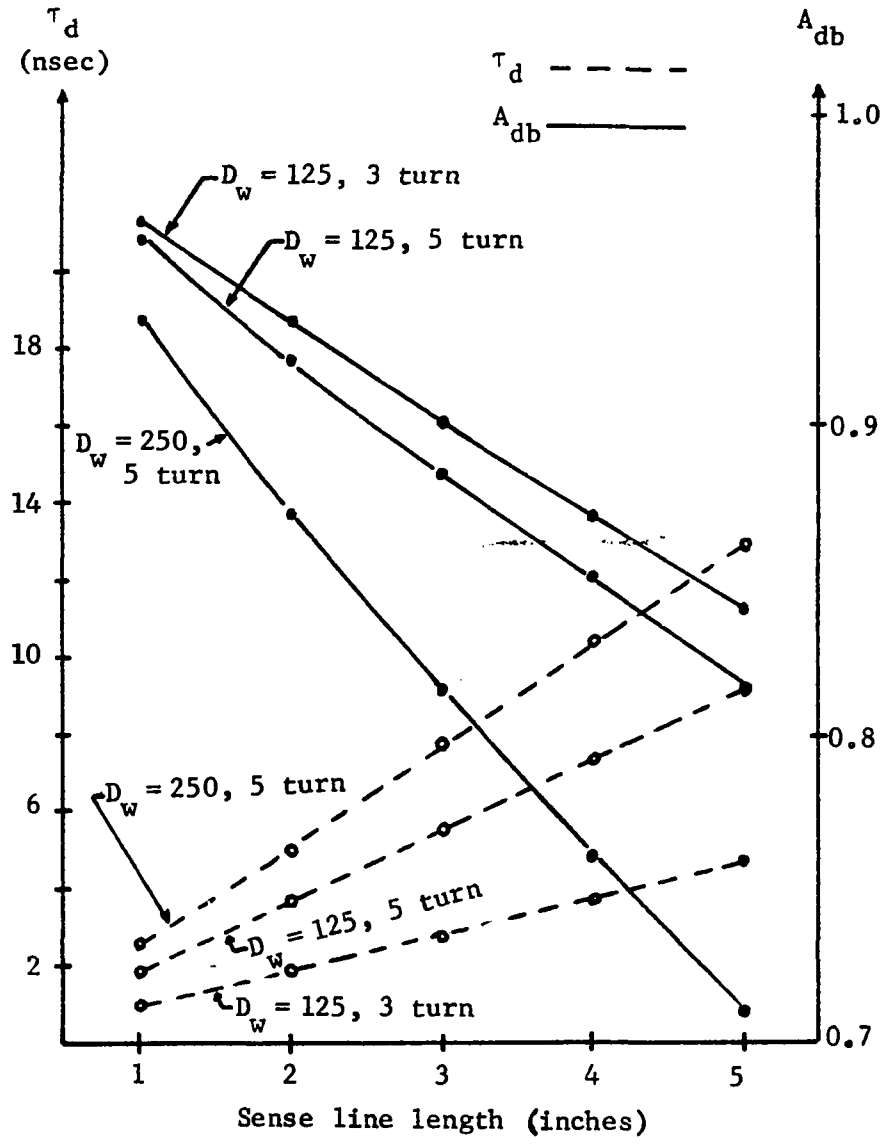


Figure 10. Down and back attenuation and time delay for the sense line

IV. DRIVE REQUIREMENTS

A. Word Line

Given: $H_K \simeq 5$ Oe. = 398 AT/M

$H_C \simeq 3$ Oe. = 240 AT/M

The word line field should be about 1.5 H_K. Then the word current required is at least:

$$H_w = \frac{1.26\ I}{2w} \quad , \quad I = \frac{7.5 \times 10^{3} \times 4 \times 2.54 \times 10^{-5}}{4\pi \times 1.26}$$

$$I = 48\text{mA}$$

A more realistic estimate of the word current is given by (27, 30):

$$H_w > H_K + 2\ H_{dh} \quad , \quad H_{dh} = 1.5\ \frac{B_s t}{w}$$

$$H_{dh} = \frac{10^{4} \times 1200 \times 10^{-8} \times 1.5}{2 \times 10^{-3} \times 2.54} \simeq 36 \text{ Oe.}$$

For the semi-closed structure in the hard direction, the demagnetization will be about 9 Oe. Thus, $H_w \simeq 14$ Oe. $\simeq 2.5\ H_K$ which implies $I_w \simeq 95$mA. This result also agrees with Kriessman and co-workers (31). Considering the fact that the word line spacing from the ground plane is high (3 mils plus) 100mA is a good estimate, 110mA was indicated by Figure 2.

B. Sense Line

With no keeper, and assuming a 2400 Å film as an approximation for the two layers separated by the copper word line, the average demagnetizing field in the easy direction will be:

$$H_{de} = \frac{B_s t}{2L}$$

where L is the effective width of the sense line. Thus for #48 wire:

$H_{de} \simeq 5$ Oe. for three turns

$H_{de} \simeq 4$ Oe. for five turns

These values of demagnetizing field would greatly shear the hysteresis loop of the material. However, one can assume a reduction in H_{de} of about 3.5 due to effective keepering. Thus,

$H_{de} \simeq 1.6$ Oe. for three turns

$H_{de} \simeq 1.15$ Oe. for five turns

If the allowed rotation of the easy axis is $\alpha \leq 3^{\circ}$, then the component in the easy direction of the word field is about 12 (Oe.) $\times$ $\sin(3^{\circ}) = 0.63$ Oe.

Trapped flux contribution from the word line will not be significant (32), so is the case with a thin ground plane (3 mil, below the film pair).

The tangential contribution of adjacent sense line can be approximated (17) by:

$$\frac{H_2}{H_1} \simeq \frac{S\,b}{.4\pi\,d^2}$$

where: s = line to ground plane distance

b = line width

d = center to center seperation

For the geometry depicted in Figure 1 the ratio is 0.016 which will be reduced to about 0.04 by effective keepering. Additional worst case configurations will be ignored for the time being.

Considering all the above contributions, the digit field for 3 and 5 turn lines should be:

(3 turn) 1.85 Oe. $\leq H_d \leq$ 2.33 Oe. (5 turn).

The digit current can now be calculated from $H = \frac{1.26\ In}{2w}$.

The digit current I_d is:

(5 turn 16 mil center) 8.5mA $\leq I_d \leq$ 13mA (3 turn 8 mil center).

V. DENSITY OF LINES

A. Word Line

Results published (24) and the calculations in previous chapters indicate that 2 mil lines on 8 mil centers are possible. There is strong evidence (24) that 4 mil centered lines should be tried. While 8 mil centered lines satisfy margin considerations (17), 4 mil centered lines might become critical.

B. Sense Line

Consider #48 wire, 5 and 3 turn lines. The 5 turn line is favored in terms of the signal obtained. The lines should be on 16 mil centers in order to safely satisfy margin considerations. For high density purposes 12 mil centered lines should be tried. The 3 turn line favored by time delay considerations should be on 12 mil centers, but 8 mil centered lines should be tried.

The range of bit density for the lines mentioned above is:

$$7750 \text{ bits/inch}^2 \leq \text{density} \leq 31{,}250 \text{ bits/inch}^2$$

While the favorable densities in terms of safe margins are:

125 word line/inch, 62 (3 turn) sense lines/inch

$\Rightarrow$ 7750 bits/inch^2

125 word line/inch, 83 (3 turn) sense lines/inch

$\Rightarrow$ 10050 bits/inch^2

VI. MEMORY PLANE SIZE

From the calculations it seems that the most suitable word line will be 10,000 Å thick, with calculated resistance of 10Ω/inch. A 10 inch long word line will have about 80% down and back attenuation, depending on the sense line turns. The line can have an element density between 62 to 83 per inch 5 turn sense lines, or up to 125 per inch 3 turn sense lines. Such a line will not exceed 10-13 nsec delay.

For the sense line length a 5 inch 5 turn line with about 10 nsec delay and 20% down and back attenuation is possible. Also to be considered is an 8 inch 3 turn line with less than 10 nsec delay and about 20% down and back attenuation.

The densities per plane are depicted in Table 10.

Table 10. Plane densities

Sense line			
Density per inch	Length (inch)	# of turns	Density per plane
62	5	5	387,000 bits
83	5	5	518,000 bits
83	8	3	830,000 bits
125	8	3	1,250,000 bits

word line
10 inches long
D_w = 125 lines/inch

Note that the L/R approximation allows only 3 turn lines for a 200-250 nsec memory.

VII. MINIMUM DELAY AND COST CONFIGURATION

If P_w and P_s are the propagation delays in the word and sense lines respectively, then it is found (17) that for a minimum cycle time memory, the number of words, N, and the number of bits per memory word, M, is given by:

$$N = \sqrt{C \frac{P_w}{P_s}} \; ; \quad M = \sqrt{C \frac{P_s}{P_w}} \; ; \quad \text{where } C = NM$$

It turns out that for a large memory, each word line should drive what would correspond to a number of words.

For a 10 inch long word line with 3 turn sense lines, 83 sense lines per inch, the one way delay is (0.0055 nsec/inch × 83 × 10) = 4.6 nsec. If the number of bits is decided upon (M = 830) then,

$$M = \sqrt{C \frac{P_s}{4.6}} = 830$$

for $C = 10^6$ $P_s \simeq 3.2$ nsec. This corresponds to a 4 inch long sense line, which in turn corresponds to 500 word lines per plane (at a density of 125 lines/inch). A word line longer than 10 inches will not be compatible with integrated circuits, thus if the longest lines (discussed previously) will be used, a minimum delay (per plane) organization will not be achieved.

However, if one is willing to increase sense line length, a geometry for a minimum cycle time memory can be obtained. With the favorable densities discussed, such a geometry will have about 1500 word lines per sense line.

Although minimum cycle time design is an attractive exercise, for large memories it is more important to obtain a minimum cost configuration. It has been predicted (33) for 1971 that large semiconductor (and core) memories will cost less than a cent per bit. For the memory to meet such a cost objective the number of word lines per sense line must be increased. It has been mentioned before that for reasonable data rates long words have to be used. In addition, it will be advantageous to trade memory speed for cost, in order to get below the 1 cent per bit cost. It turns out that the number of word lines per sense line will have to be at least 8000 so a sense+digit electronics cost in the 0.1 cent region can be obtained. Such a configuration is essential for a low cost memory.

If one has a 8192 bit long sense line with 125 bits/inch then a 65 inch long line will result. This line can be halved for noise cancellation. A quick check with the previously demonstrated calculation shows that such a line will not have favorable characteristics. In order to obtain more attractive characteristics and keeping the low cost objective in mind, one can use two substrates back to back doubling the number of bits per sense line. The previously calculated parameters can be easily modified to accommodate the new structure. For 8192 words per sense line, or 4096 for a halved line, the length of the sense line will be 16.5 inches (or about 100 inches of #48 wire for a 3 turn sense line). The characteristics of such a line are summarized below:

$R_{DC} \simeq 50\Omega$

Inductance $\simeq 97 \times 10^{-12}$ henry/mil

$Z_o \simeq 72\Omega$

$\tau_{db} \simeq 40$ nsec

$A_{db} \simeq 50\%$

If one assumes: (17, 34)

1) A plane of C bits, organized into N words of M digits, each represents a fixed cost regardless of the choice of M and N.

2) Word selection cost is assumed to be linear with N, with an associated word cost D_W.

3) Digit electronics cost linear with M, with an associated digit cost D_S.

Then to minimize total cost:

$$N = \sqrt{C \frac{D_S}{D_W}}, \qquad M = \sqrt{C \frac{D_W}{D_S}}$$

Under this simplifying assumptions:

$$C = 600 \times 8192 = M \times N = 4{,}915{,}200 \text{ bits/plane}$$

The sense+digit cost equals 13 times the word cost. If such a ratio is maintained, a good cost minimization can be obtained.

VIII. THE SPUTTERING PROCESS

A. Introduction

Since its discovery in 1852 by Grove the various techniques (35) of the sputtering process attracted the growing interest of researchers and industry alike (36).

The films for the study presented in this thesis were prepared by RF sputtering. RF sputtering has been used primarily for the direct sputtering of insulators. The use of RF sputtering for this purpose has been reviewed by Davidse (37), however, it is also possible to RF sputter metals. Relatively high rates can be obtained, and films are of very good quality because of the low pressure at which the RF glow discharge can be operated. Some of the advantages of the sputtering process are listed below.

a) Complicated materials such as Evanohm and Permalloy can be sputtered without composition changes.

b) Film thickness control is simple once the deposition rate is determined. Thus, film can be reproduced well.

c) Cleaning of the substrates is simple because surfaces can be sputter-cleaned.

d) Since the process is not thermal (evaporation) but a process of removal of atom layers, targets can be used for a long time.

e) Greater film thickness uniformity.

f) Since this is an atom by atom process highly polished surfaces can be obtained.

g) In combination with photo resist one can sputter etch without undercutting and achieve fine pattern resolution, even for materials which are difficult to etch by chemical methods.

Despite great experimental work, the development of the theoretical understanding of sputtering has been slow. Present day sputtering theory generally considers the mechanical collisions occurring between the impinging ion and the target atoms. It is believed that the atoms sputter as a result of surface collisions involving about four atomic layers which eventually leads to the departure of atoms from the target.

The equipment required for sputtering varies with the method used. The equipment used for RF sputtering as related to the work presented in this thesis is described below.

Two RF generators are available, both feature a 120 watt exiter, a 1 kWatt amplifier and a match box with a directional coupler providing forward and reverse power measurements. The generators are for 27 and 3.5 MHz. The former is used for the RF excitation of the plasma, while the latter is used with dilectric targets including RF etching.

Two independent RF excitation modes are available. One is an externally mounted double loop antenna like structure made of 50Ω Teflon coaxial cable. The other is an inner-loop which is located inside the vacuum chamber. This loop is water cooled and is excited by a balanced double ended line. Using this loop provides one with higher sputtering rates, an even faster rate can be obtained by a method mentioned later.

In addition a DC field is applied via an external pair of Helmholtz coils driven by a 50 volt, 30 amper power supply. A 1 kVolt 500mA DC power supply is used for the DC potential connected to the target.

The vacuum system features a six inch oil diffusion pump, liquid nitrogen trap, mechanical pump, glass bell jar, target assembly, feed-through ports and an argon source.

The glass bell jar offers an effective 10 inches in diameter 10 inches high cylindrical working space. Top and bottom Microy plates offer good mounting surfaces for various holders as well as good insolation from top and bottom stainless steel plates.

The target assembly offers a great deal of versatility. Two independent target assemblies are available. The inner-loop can be used for direct sputtering. When this loop is also used for excitation very high rates are possible. The other target assembly is a multiple target device which enables one to sputter up to four different materials without breaking vacuum. This target assembly is set by rotation, then the appropriate target is lowered into the center of the working space. In order to switch targets the used one has to be pulled out, the assembly rotated and a new target lowered. A diagram of the sputtering station is depicted in Figure 11.

During sputtering the chamber is backfilled with argon through a micrometer needle valve. Feed throughs can be used for cooling and heating substrates, shutter assemblies, measuring probes or for any other purpose one desires.

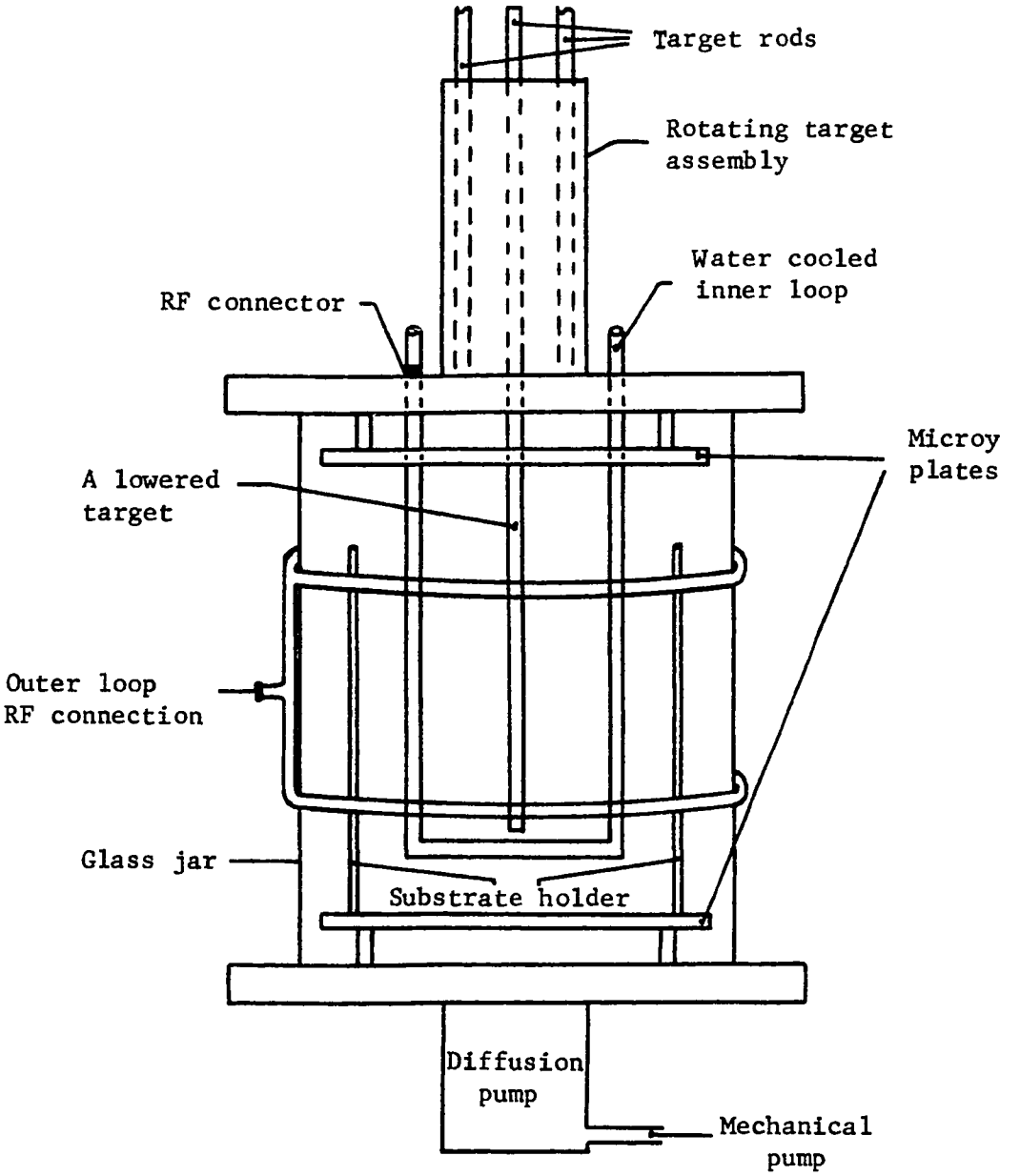


Figure 11. Sputtering station diagram

B. Device Fabrication

The sputtering process proved to be one of basic simplicity. Improvements in technology (38) have changed the bad reputation sputtering acquired for nonreproducible results. Sputtered films show parameter behavior similar to evaporated magnetic films (39). However, the sputtering process is highly reproducible.

Before a device can be made the deposition rate needs to be determined. The system described in this thesis was calibrated by inserting a crystal in the vacuum chamber. The frequency shift (measured after sputtering) was used to determine the thickness of the material sputtered. A change in sputtering rate is achieved by changing the DC voltage and current applied to the target rod. In addition a substrate heater was inserted and calibrated by a thermo-couple attached to the substrate holder. Magnetic properties of Permalloy films are highly dependent on temperature variations and underlayers. The general correlations observed were very similar to the ones compiled by Mayer (39).

The device described in this thesis was sputtered on a 3 mil glass substrate. These substrates were cleaned ultrasonically and degreased before insertion into the system. The glass jar was cleaned in acid and baked before usage. The system was pulled down to 1.5×10^{-6} torr overnight. During this period, the system was baked at $150^{\circ}C$ using the substrate heater. It should be noted that vacuum measurements were made by an ion gauge located 10 inches below the chamber. Thus, it would be

reasonable to assume that the vacuum in the chamber was higher by an order of magnitude.

Sputtering was done by using the inner-loop which is easier to control than the outside one. The inner-loop is only slightly affected by screening, and sputtering current control is simple. Before sputtering the system is back filled with argon at a pressure of 10^{-3} torr. Eight glass substrates and a smaller sample substrate were used per run. These substrates measure 3.6 X 1.7 inches and 0.867 X 0.867 inches (22 X 22 mm) respectively. The RF power was maintained at 850 watts for all materials.

Table 11 below represents a summary of the materials, thickness, and rate used for the memory device.

Table 11. Target materials and sputtering constants

Target material	Thickness Å	Sputtering current density mA/cm^2	Target potential DC volts
Chromium	200	9.8	200
Permalloy	1,200	8.7	550
Copper	10,000	4.1	350
Titanium	400	8.7	300
Permalloy	1,200	8.7	550

The copper underlayer represents one of the more critical depositions. As mentioned previously, it is desired that the top Permalloy layer will have the same properties as the first one. Copper underlayers tend to increase H_c (20, 40). To rectify this problem, the substrate was water cooled during the sputtering of copper. In addition, a cooling period of half an hour followed the deposition of copper after which a layer of 500 Å of Cu was sputtered followed by 400 Å of Ti as additional smoothing.

Figure 12a shows the easy and hard direction loops of a single layer film. Figure 12b and c show the double layer film with and without smoothing.

It should be noted that film properties can be improved substantially. Better cleaning procedures and cocling system need to be used. The most important control one has, particularly in soft films, is temperature. To that end, it will be advantageous to preheat the system before sputtering and let it cool to the desired temperature. In the system described it was not possible to reach temperatures higher than 200°C. For thickness uniformity a shutter should be used. This shutter should be opened only after the target and chamber reach a steady state temperature. Better vacuum techniques should be used. A liquid nitrogen trap and a bent vacuum system are essential to avoid back streaming.

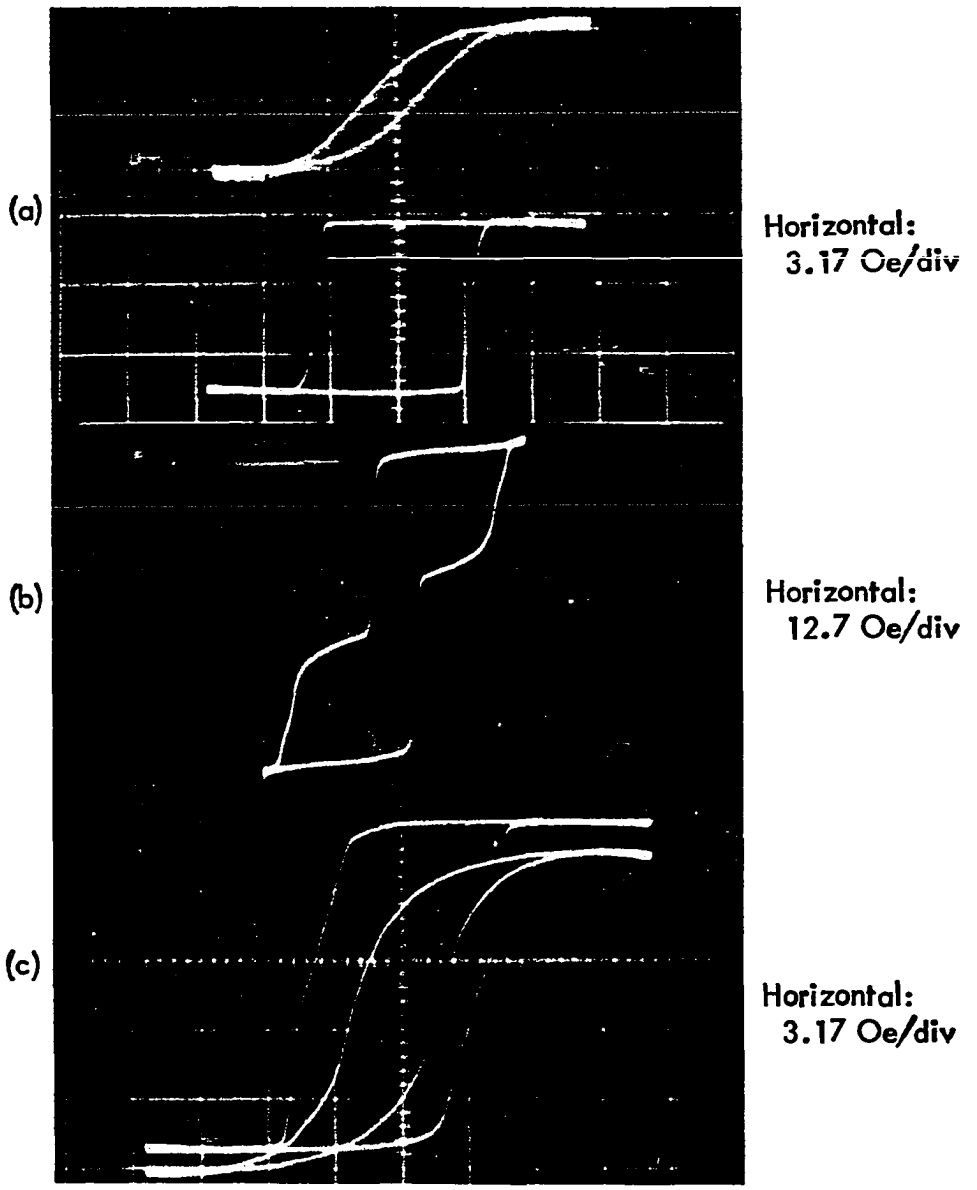


Figure 12. Hysteresis loops
(a) Hard and easy loops for a single 1200 Å layer
(b) Easy direction loop for a coupled film without smoothing
(c) Hard and easy loops for a coupled film with smoothing

The films described above are continuous. In order to make use of these films, the word lines need to be etched. Consideration was given to sputtering through a mask in order to avoid etching. However, the masking technique requires perfect mechanical contact between mask and substrate. Furthermore, this method often produces tapered lines such as described by Pohm and co-worker's report (24) where asymmetric write currents were observed. This is partially due to edge domain formation in the hard direction. When an etching method is chosen one needs to consider under-cutting (edge problems) and definition. Chemical methods become complicated when a wide range of materials must be etched (and such is the case here), and result in considerable under-cutting. The complexity and under-cutting associated with chemical methods result in poor control over line width. Various methods are available using electrolytes with the sample used as a cathode or an anode. These methods, in addition to under-cutting leave a bottom layer of islands which cannot be etched as current ceases to flow. Futhermore, contacts to a current supply need to be provided, which makes handling more difficult.

The most suitable method for the application called for in this thesis is the sputter etch one. This method, as the name implies, uses the sample to be etched as a target. The area which need not be etched is protected by a layer of photo resist just like in the other methods mentioned above. The photo resist is etched away with the other materials. However, its relative thickness protects the covered areas.

A mask was prepared using #44 wire (0.023 inches in diameter). One half of the mask has wires on 7.8 mil center while the other on 3.9 mil centers. With under-cutting, during exposure of the photo resist the line width should be close to 2 mil and the center to center distances close to 8 and 4 mils. The magnetic film substrate was covered with a thick layer of Shipley AZ-111 positive photo resist and baked to improve adherence. After exposure and development the sample is ready to be etched.

The same sputtering station described previously is used for the etching process. The plasma excitation is done via the outer-loop at 27 MHz. The sample is placed on a greased copper table six inches in diameter. This table is water cooled and connected to the 3.5 MHz transmitter. The RF potential on the target is needed since the film is deposited on a dilectric (glass). After the sample is placed on the copper table the exposed areas are shielded with glass so the table will not be sputtered. With 800 watts output on both transmitters it took on the average 1.5 hours to etch through 14,000 Å of film. Faster etching rates can be obtained. However, care must be taken not to burn the photo resist or overheat the target. Figure 13 shows the high density area of an etched sample. The dark areas represent the word lines, the light areas are regions of clear glass. The picture was taken by a scanning electron microscope and clearly shows the top (rough) protective layer of titanium (sputtered on some samples) after rubbing off the photo resist. The average line width is 2.2 mils

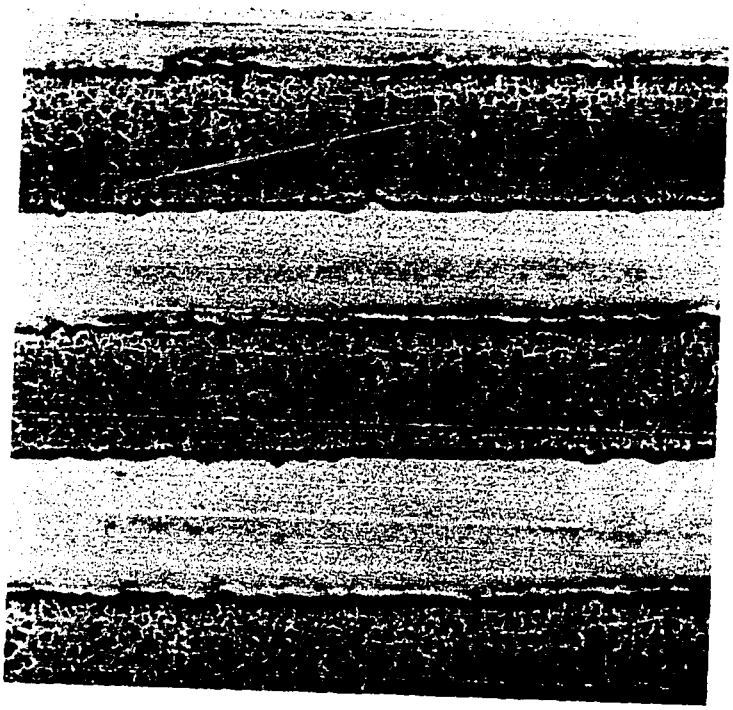


Figure 13. High density area of an etched film
Magnification: 300

(not as much under-cutting during exposure as expected), and the average center to center distance is 4.2 mils. The darker regions along both sides of the etched lines are 28,000 Å wide on the average. These dark strips, when considered as evidence of tapered edges, represent a slope of about 33°. However, closer examination of over etched samples, and the low density area which is etched faster, points out that the side walls are very steep. The dark strips represent an unetched area of the bottom chromium layer which extends about 28,000 Å beyond a well defined word line. In the low density area these dark strips are almost nondiscernible.

IX. MEMORY ARRAY

A. Partially Populated Device

A partially populated DRO memory plane representing over 2×10^6 bits was constructed to demonstrate that the developed DRO storage element can be used in a main store memory. The element structure is the same as depicted in Figure 1. However, the Mu-metal sheet is replaced by an element identical to the one above the ground plane. The principle of the back to back substrates is shown in Figure 14A. The plane was fabricated so tests can be performed on various line densities. Word lines were sputter etched on 7.8 and 3.9 mil centers. Sense lines were wound with #44 wire (3 turns each) on 12.2 and 8.5 mil centers. The plane is so constructed that a two location per bit arrangement can be also tested.

It should be noted that all densities feature the same line lengths. Thus, when word lines and sense lines are on 3.9 mil and 8.5 mil centers respectively, the memory capacity is about 2.5×10^7 bits. Sense lines are constructed in an alternate fashion, i.e., inputs and outputs alternate for better signal to noise ratio.

Figure 14B shows the partially populated memory plane. As shown, the fabricated bits are located at the input and output ports of both sense-digit and word lines. There are four sense lines for each density, or a total of sixteen lines. Ferrite Keeper was applied to the populated area. Ferrite powder was mixed with rubber cement and diluted with a rubber

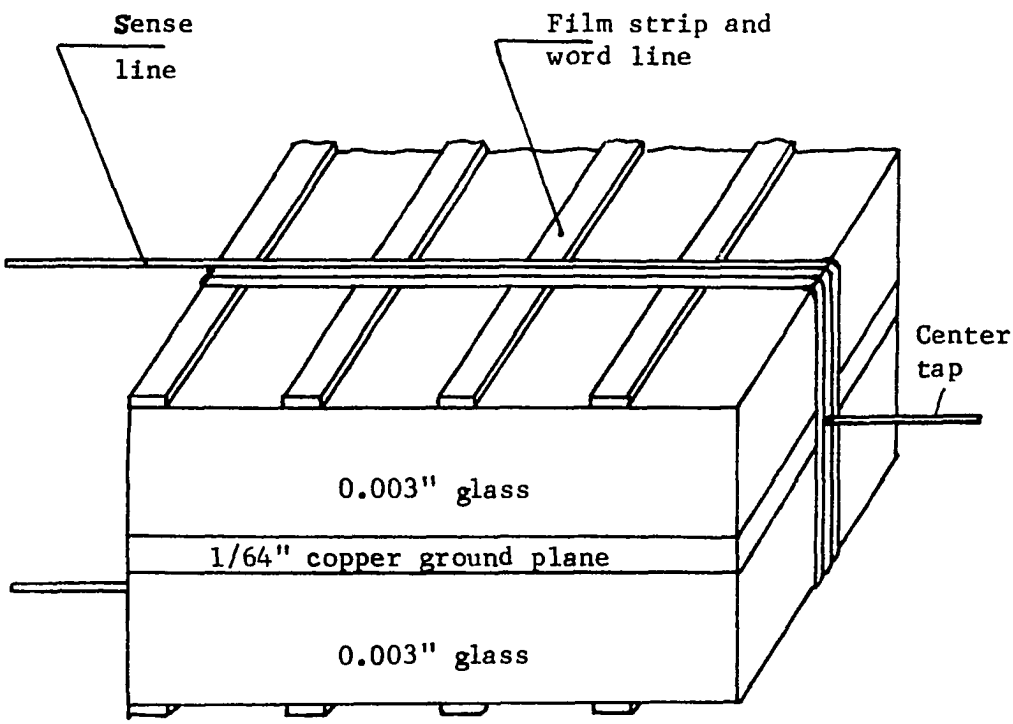


Figure 14A. Basic construction of the memory plane

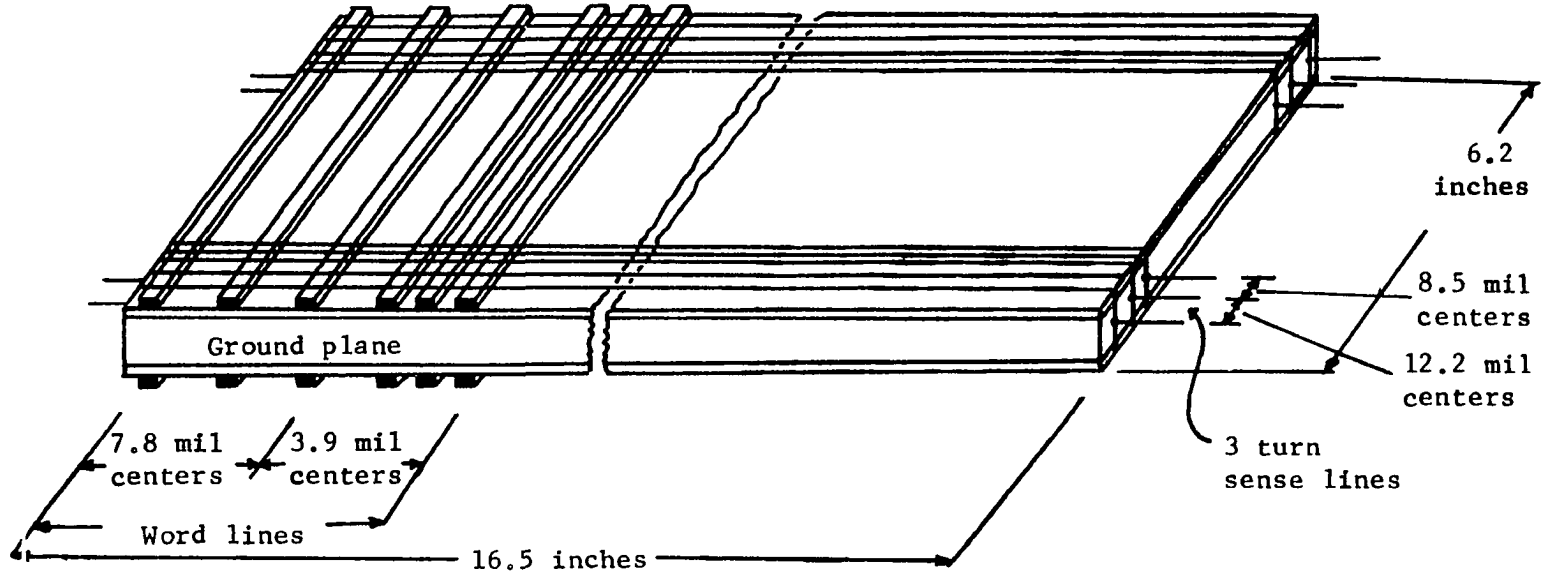


Figure 14B. Partially populated memory plane

cement solvent. After the Keeper is poured on the memory the solvent evaporates and the Keeper solidifies.

The components used for the peripheral electronics were as designated by subsequent figures. All integrated circuits used were of Fairchild's TTL family.

B. Word Line Selection

Word line selection is based on 256 packages. Each package, as demonstrated by Figure 15, is connected to 32 word lines. Upon decoding the proper portion of the address field, one IC Select line is activated with one base via the 5 bit decoder. Upon termination of the Dummy line one of the word lines in the group of 32 is selected. The Dummy line controls a transistor switch which reduces read noise by reducing word selection transients. A sample of the read current and the Dummy signal is shown in Figure 16.

C. Digit and Sense Electronics

The basic arrangement of the sense and digit electronics is shown in Figure 17. Although transformer coupled digit drivers offer some advantages, the disadvantages of cost and transformer recovery disqualified them for this design. Two preamplifiers are connected to each sense amplifier, however, only one preamplifier is activated at any given time by the proper decoding of the Address bit. The sense amplifier is strobed appropriately to allow the output register to attain its ONE or ZERO state and allows the digit driver to switch in the desired direction for the

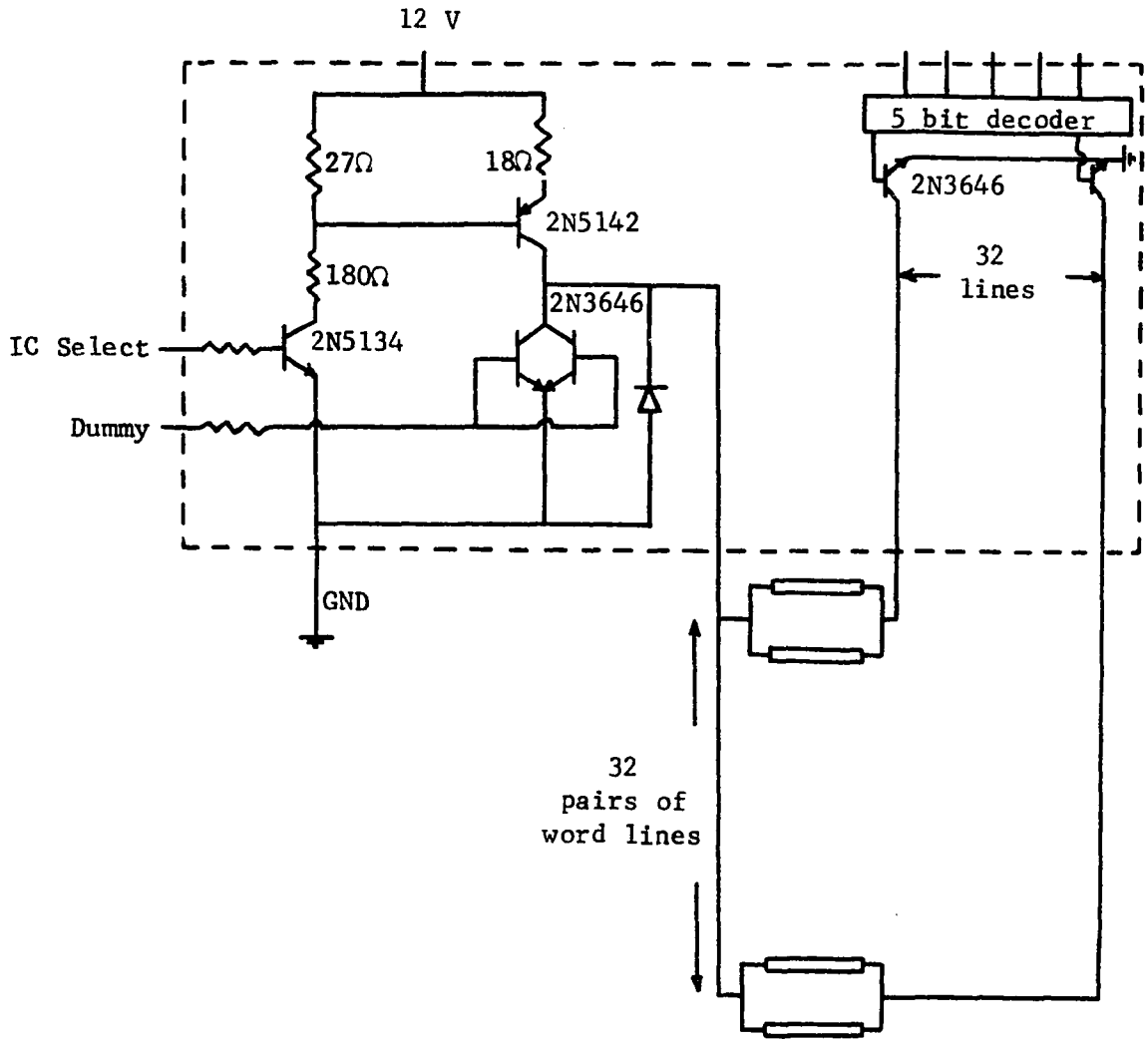


Figure 15. Word line selection package (WDM)

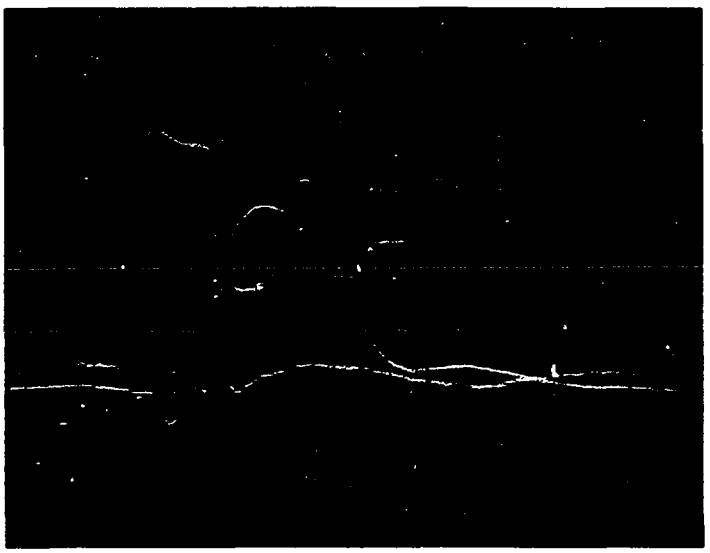


Figure 16. 100 mA word current with Dummy signal preceding it

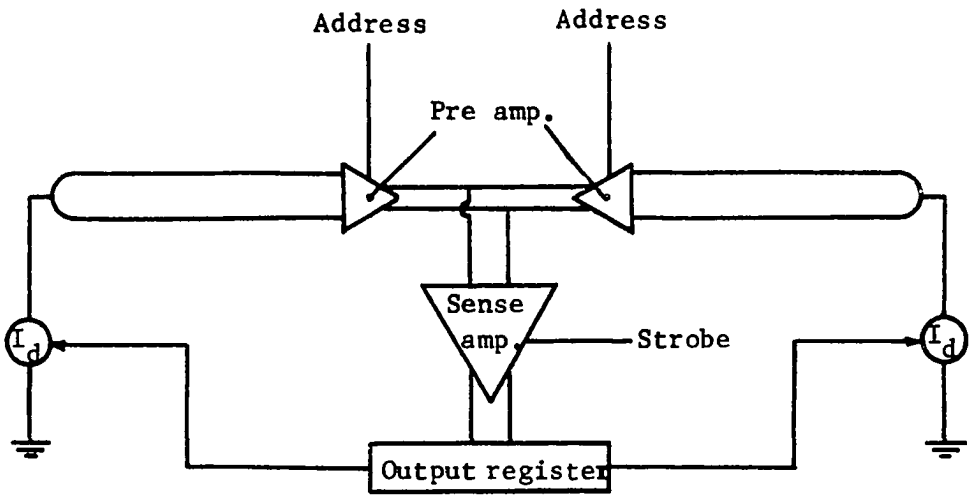


Figure 17. Digit and sense electronics block diagram

write cycle. The digit driver obtains its switching signals from the output register and will give a positive or negative (or bipolar) digit current. For noise reduction, the sense-digit lines are so constructed that a center-tap serves as an input port for the digit driver.

The sense amplifier is shown in Figure 18, also shown are the data register and the strobe circuit. When one of the two preamplifiers is selected an emmitter current source is provided. When the strobe is applied the input of the data register is raised to about 1.8 volts, enabling the register to assume its proper state. The amplifier depicted in Figure 18 has a gain of about 1000. The transistors used, except the last stage (RCA 3046), were not matched. Such a mismatch can be removed by trimming the 10Ω emitter resistors. Even with trimming, loss of gain, increase of recovery time and digit noise can be observed.

Figure 19 depicts the strobed sense signal and the content of the output register.

The digit driver is a simple bipolar switch. The circuit is so designed that unipolar and bipolar digit currents can be utilized. The digit driver is depicted in Figure 20. Test results for the two modes are shown later. Figure 21 shows the read current, digit current and the sense signal.

The timing diagram depicted in Figure 22 shows that after a Dummy signal is initiated a new cycle can be started in less than 500 nsec. It takes the sense amplifier 200-300 nsec to recover. However, this can be reduced when an IC is designed and properly placed on the memory

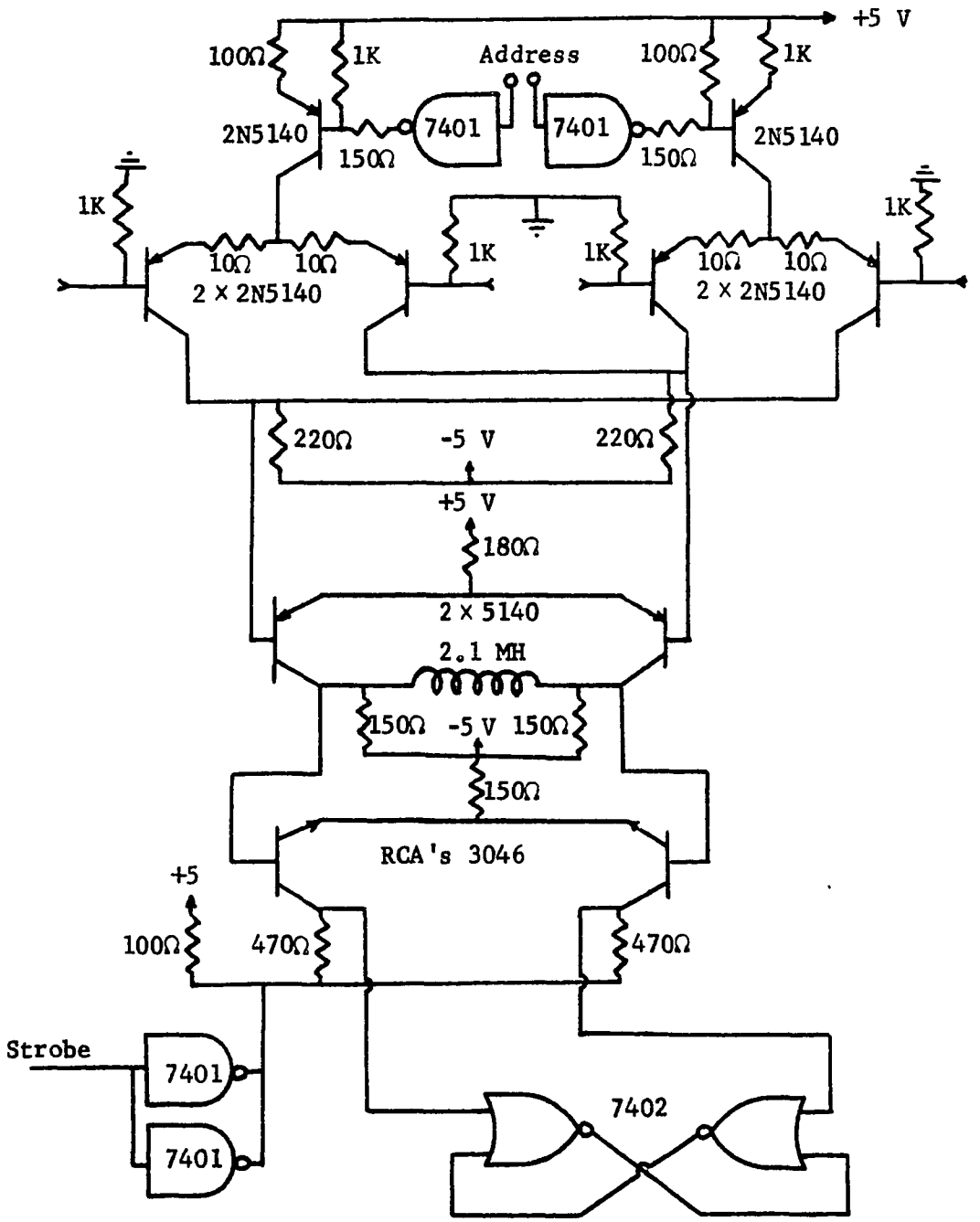


Figure 18. Sense amplifier

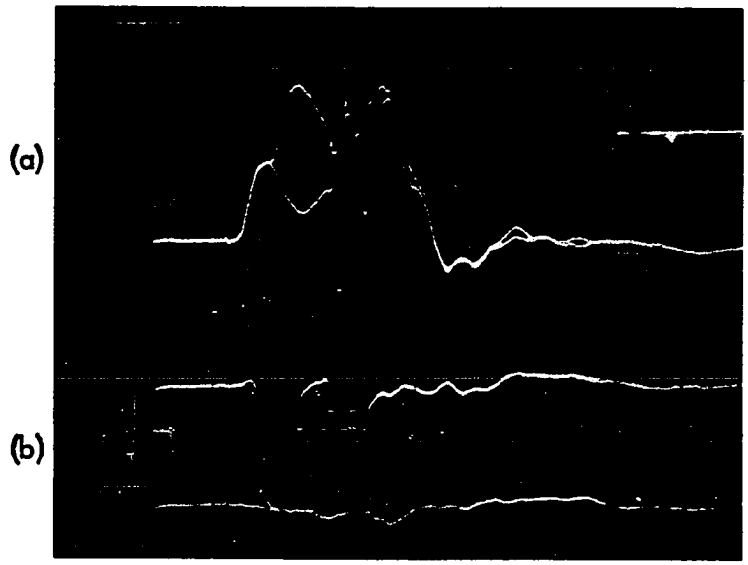


Figure 19. Output signals
(a) ONE and ZERO strobed sense amplifier output
(b) Content of output register

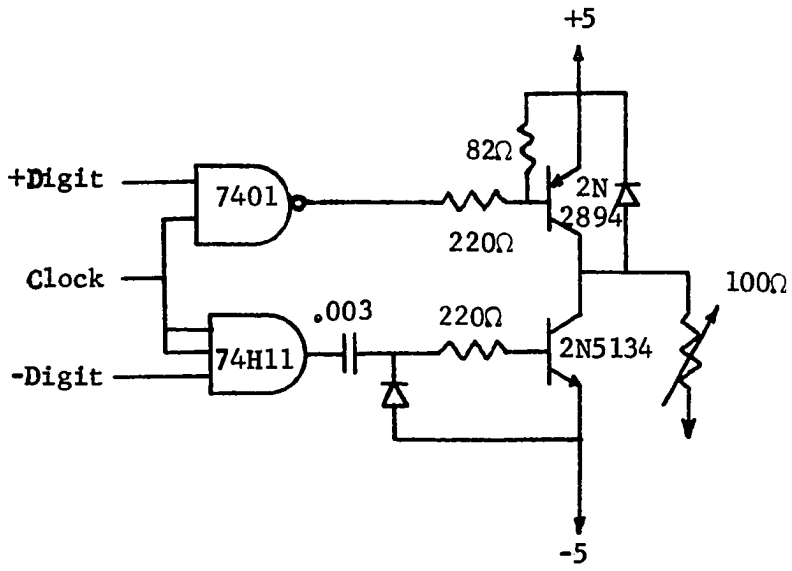


Figure 20. Digit driver

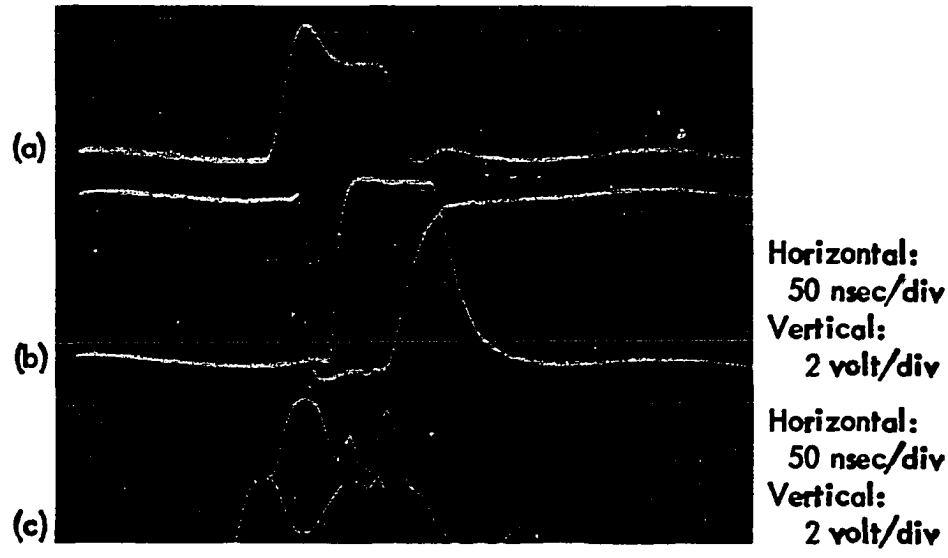


Figure 21. Read write cycle and output signal
(a) 110 mA of word current
(b) Positive and negative digit drive with negative pulse displace to the left
(c) ONE and ZERO strobed sense amplifier output

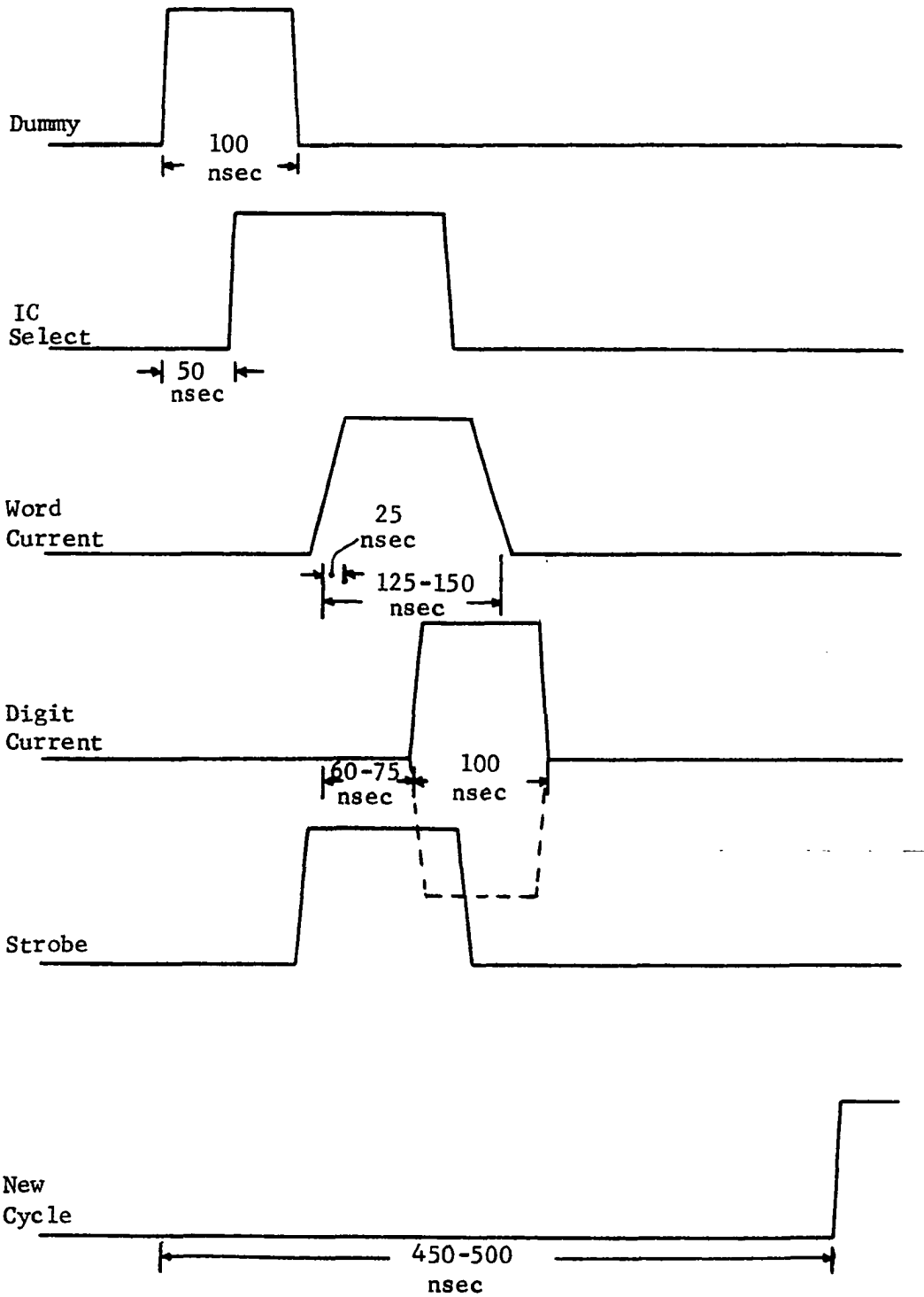


Figure 22. Basic timing diagram

plane. With the best sense amplifier built for this memory, and exercising a bit at the far end of the sense line (middle of the line), a cycle time of 400 nsec was achieved.

D. A Fully Populated Device Description

It is not the intention of this thesis to investigate the fabrication problems of the fully populated memory. However, it is obvious that one of the important cost contributions are the device interconnections. The number of interconnections can be kept at minimum if a bus system and special integrated circuits are used.

The memory stack described below went through several stages of development before the number of interconnections and IC packages were acceptable in number and size. The principle of the back to back substrate arrangement is depicted in Figure 14A. Figure 23A shown below describes partially the construction of the fully populated device. There are four basic planes (modules), each has 512 sense lines, and 2K word lines on each side. The physical size of such a module depends on the line densities and will range from 6.2 to 4.1 inches for the word lines and 16.5 to 8.2 inches for the sense-digit line. The above line lengths are for the densities mentioned previously.

The word line selection and sense-digit electronics were designed so special integrated circuits serving as functional units can be fabricated. Such circuits, as mentioned before will help to reduce memory costs.

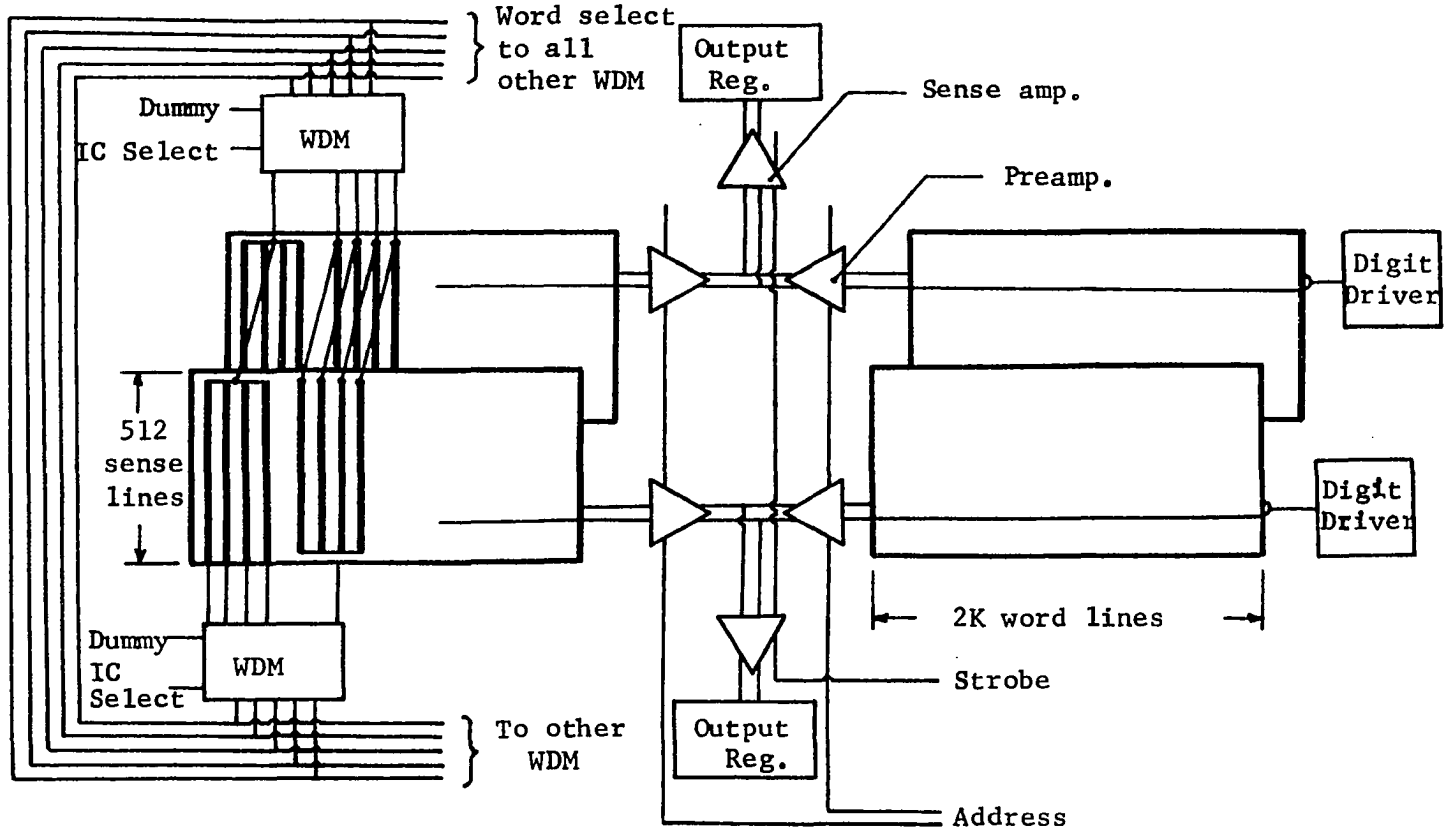


Figure 23A. Construction of the fully populated device

The word lines are grouped together into selectable groups each comprised of 32 lines. Such a group is fully serviced by one Word Driver Module (WDM) which includes a word driver and a 5 bit decoder with 32 switches for selection of a specified line. The special integrated circuit WDM depicted in Figure 15 is a 42 pin package. The pins are: IC select, which will select one out of 256 packages, 33 word line connections, ground, 12 volt supply, 5 word line select lines, and a Dummy line. The word lines are connected in an alternating fashion to ease fabrication and for better noise reduction. For such a construction a WDM module will in effect serve two word line groups as shown.

The sense-digit circuits shown in Figures 18 and 20 can be packaged in any number of ways. The sense amplifier is usually more critical because of the need for matched transistors. For a single sense-digit package a 14 pin package is needed. This kind of package will probably be the same as the dual in line IC circuits now in common use. Since 7 pins out of the total of 14 are common to all circuits it might be expedient to design a special, larger package. If the previous 42 pin package is used it might be possible to fabricate 5 sense-digit circuits in one IC package. Figure 23 does not show the sense-digit electronics as a single package, however, the principle should be clear.

The number of interconnections, as mentioned before, can be reduced by using special integrated circuits and a bus system. It can be shown that with the IC packages discussed above and a bus system (discussed later), a 45% reduction in connection is realized as compared with a direct matrix method ($2^6 \times 2^7$) and dual in line (14 pin) packages.

The memory is serviced by several buses. A five line bus for the word line selection, eight bit bus for the selection of a WDM (IC select) and a Dummy line. The supply bus has three lines, +5 volts, -5 volts, and a 12 volt line. For the sense-digit electronics the memory requires a two bit bus for the preamplifier selection and a strobe line. A main clock and ground lines complete the list. A 22 line bus system will provide the memory with all its selection and timing signals.

E. Cost Estimates

It would not be unreasonable to expect an overall cost of 0.2-0.5 cent per bit for the fully populated memory. Of course, a large economic commitment would be required for a large scale production.

One can assume an overall cost which equals 2.5 times the direct manufacturing cost. Based on this assumption, a rough estimate indicates that a cost of 0.25 cent per bit is reasonable.

1) Electronics cost.

Assume \$2.00 per package for the Word Driver module	$2 \times 256 =$	\$ 512
Sense-digit integrated circuit at \$5.00 per IC	$5 \times \frac{1024}{5} =$	\$1024
Control logic		\$ 500
Power supply (+5V, -5V, 12V) assume \$6 per A for 5V supply and \$15 per A for 12V supply		\$1500

2) Printed circuit boards for sense-digit, WDM and other control logic electronics, including testing.

Assume \$1 per package	\$ 600

3) Substrate processing and testing.

For a 6.2 x 5.5 inch substrate (24 will be needed), including materials should not exceed $25 assuming 2 hours per 2 substrates. If one assumes 50% yield then the cost is: $4 \times 24 \times 50 = \$4800$

4) Connections.

Sense line and word line connections assuming 1¢ per point	$ 150
Stack connectors at 15¢ per pin	$ 30

5) Stack assembly (based on GE Report (5)).

Labor	$1000

6) Sputter etch.

Assuming one hour per substrate including photographic work should not exceed $10	$ 240
Thus, the total direct manufacturing cost is	$9800

or less than 0.1 cent per bit.

It should be noted in item 3 that the figure is based on two substrates per run, thus, producing a high substrate processing and testing cost. A production line sputtering station will have to process at least 6-8 substrates per run to be economical.

F. Array Test Program

The performance of the partially populated memory was evaluated by testing bit and disturb characteristics. There are 24 individual bits available for bit tests and 4 for disturb test for each density. The following tests were performed:

1) Line characteristics were measured, including transmission line properties with an hp 1415A Time Domain Reflectometer.

2) Write threshold--digit current versus word current which correspond to a successful single write operation. Creep threshold for 10^7 disturbs corresponding to 80% signal.

3) Read curves--peak signal at the output of the sense amplifier verses word current.

4) Element disturb characteristics.

This test program consists of five sequences:

a) Pre-write

b) Set

c) Write

d) Disturb

e) Read

Figure 23B depicts the test sequence. During the Pre-write sequence the bit under test (W_i, b_j as shown in Figure 23B) is saturated by 10^3 write operations in the direction opposite to the desired information state. This sequence ensures maximum bit spreading.

The Set sequence consists of 10^3 write operation. The digit current is applied on the same bit line as the bit to be tested with W_{i-1} and W_{i+1} activated in regular coincident fashion. This ensures that the static field will oppose the writing field to be applied to the tested bit. This sequence should allow the tested bit to reach equilibrium flux enclosure pattern, so maximum demagnetizing field will be established.

During the Write sequence adjacent bit lines are driven (b_{j-1}, b_{j+1}) in such a way so their stray field opposes the writing bit field. At this time bit $W_i b_j$ is also written into the desired direction. The net field observed by the tested bit will be approximately equal to the bit pulse minus the stray field from the adjacent bit lines, the static field from the adjacent bits, and the demagnetizing field from its own trapped flux during switching.

The Disturb sequence is designed to destroy the written information by domain wall creep. 10^6 write operations are executed by alternating between W_{i+1} and W_{i-1} in such a direction as to destroy the written information in the tested bit.

After a pause to allow for transient relaxation, the tested bit is read once during the Read sequence and the output of the sense amplifier recorded.

In order to compensate for circuit and film characteristic variations, the set and write sequences are done with currents 10% above normal. The disturb currents are 10% above normal. It is believed that such margins will adequately demonstrate average characteristics.

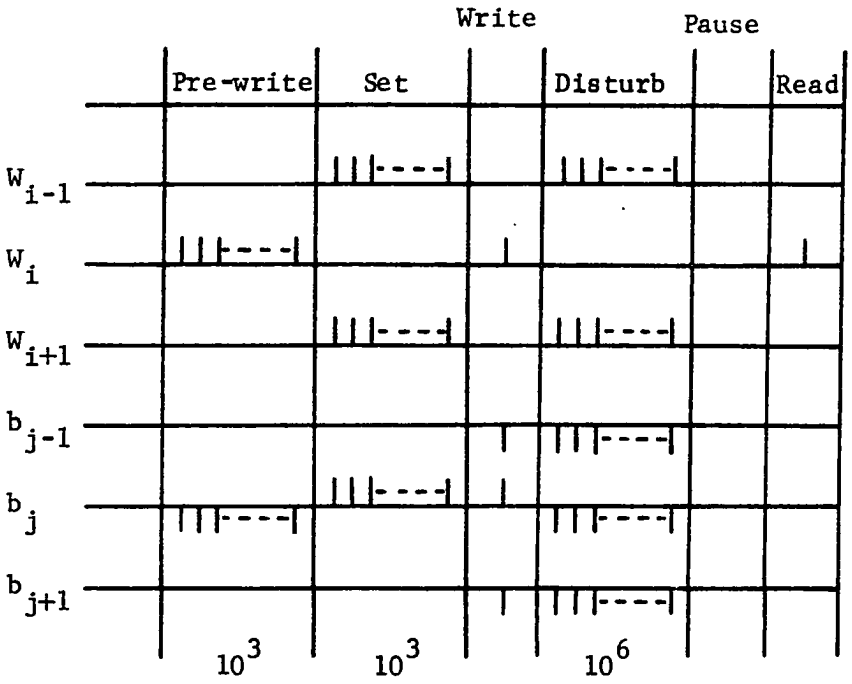


Figure 23B. Test sequence for worst case

a) Pulse pattern for tested bit $W_i b_j$
b) Stored information

G. Test Results

Some of the sense-digit and word properties were measured and are summarized below:

Word line:

Length 6.75 inches

DC resistance 80Ω which is about 22% higher than the predicted resistance. This can be attributed to thickness variation and differences in resistivity

Down and back delay about 8 nsec

Sense line:

Length 16.5 inches

DC resistance 23Ω

Down and back delay from the center of the line 24 nsec

Characteristic impedance about 100Ω

Line inductance 5.2 μH

The worst case difference between the predicted and the measured value is 22%.

The properties of the sense amplifier are evident from the previously demonstrated results. In addition Figures 24 and 25 point out additional recovery and signal characteristics.

Figure 24 demonstrates that the sense amplifier's recovery did not change much when the strobe was disabled. The increase in recovery when the strobe is disabled, is proportional to the increase in digit noise. It should be noted that digit noise is comparable to the signal and needs to be reduced.

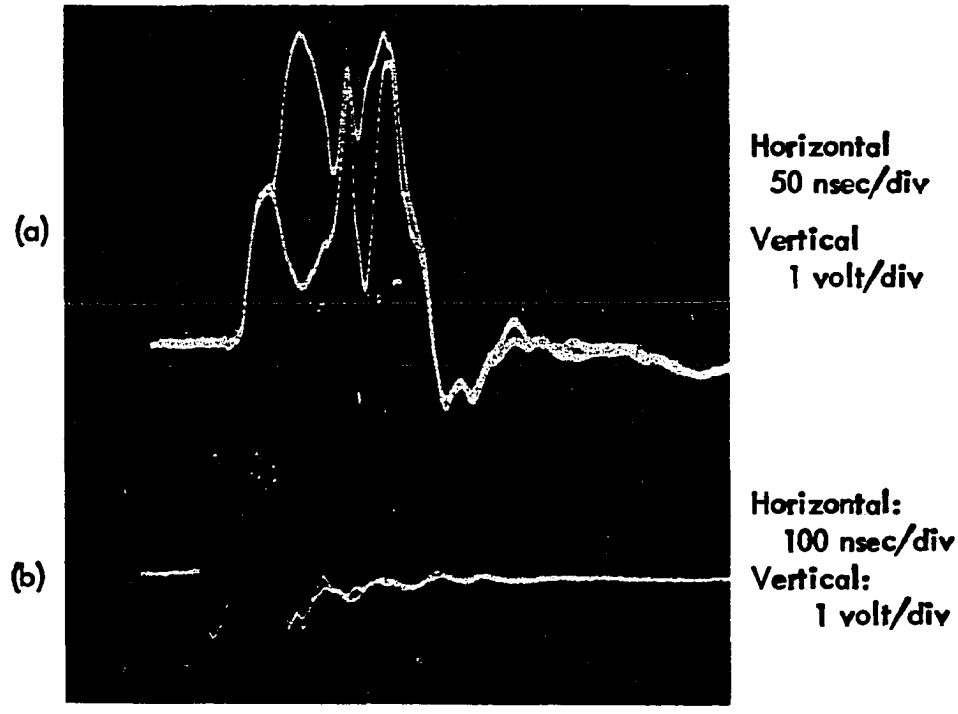


Figure 24. Sense amplifier output
(a) ONE and ZERO output with strobe
(b) ONE and ZERO output without strobe

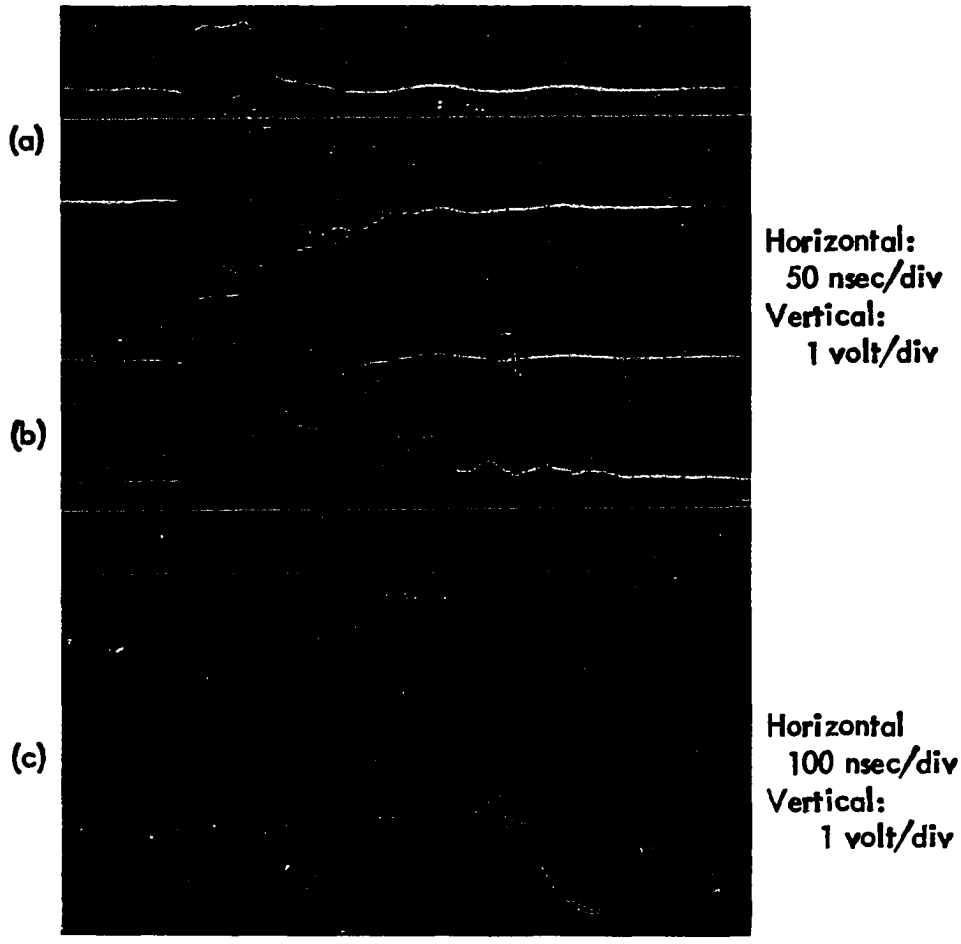


Figure 25. Sense amplifier recovery
(a) To a unipolar 12 mA digit drive
(b) To a bipolar 12 mA digit drive
(c) Burst of memory cycles

Figure 25a and b show the amplifier's recovery to the digit driver. The 1.5 volts peak to peak response was measured at the output of the sense amplifier. Great attention was given to the balancing of the first stage. However, all stages need to be balanced in order to reduce this noise. It was observed that even with a matched last stage IC package, a 35% increase in peak noise was observed when a package was replaced. On the average, the recovery time never exceeded 250 nsec. However, this was achieved after numerous transistors were tried. Not all the amplifier's components were close enough to ground, and the layout of the amplifier left much to be desired. It is assumed that such problems will be rectified when an integrated circuit is designed. The burst of memory cycles, as demonstrated by Figure 25c, shows the best results obtained which correspond to a cycle time of about 400 nsec.

Typical threshold characteristics are shown in Figure 26. The difference between the ONE and ZERO write threshold can be accounted for by skew. It is believed that most of the skew is in the magnetic film itself. The contribution of the mechanical placement of the substrate and the sense line windings should be very small. A great deal of care was taken during etching, placement of substrates and sense line construction to keep the lines properly aligned.

The read curve shown in Figure 27 demonstrates that almost double the signal is available for a two locations per bit construction. However, it should be remembered that such a construction halves the memory capacity. The output signals measured at the sense amplifier's

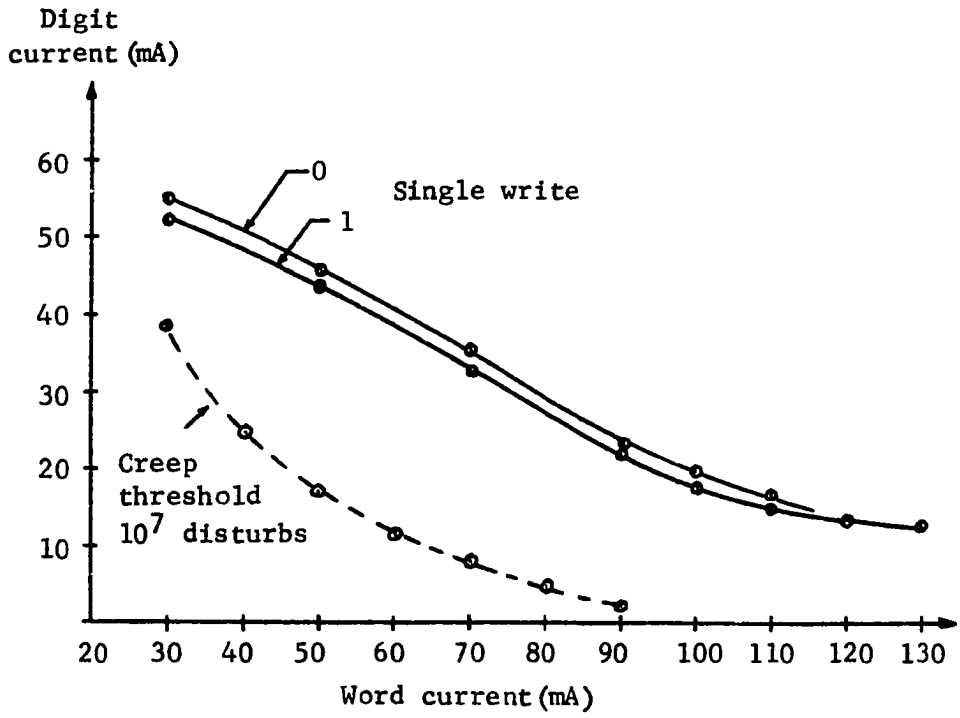


Figure 26. Typical single write and creep thresholds

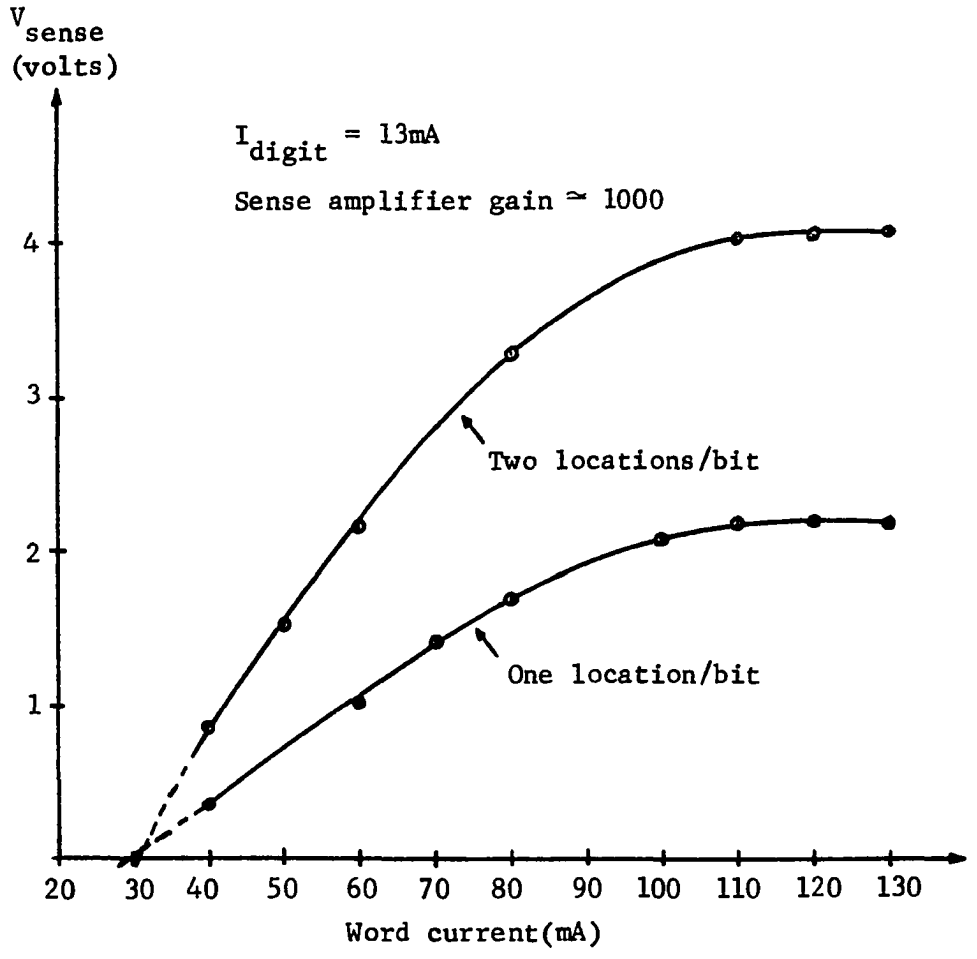


Figure 27. Read curves for one and two magnetic locations per bit

output represents a sensed signal of about 1/1000th of the measured output.

Figures 28 through 31 demonstrate disturb characteristics of various densities. The effect of skew observed previously is also observed in all of these results. However, the effect of edge domains observed by Pohm and co-workers (24) is not observed here. This is attributed to the fact that the sputter etching method used results in steep walls rather than tapered ones.

All tests performed included unipolar and bipolar digit disturbs. Because of the semi-closed hard axis configuration, adjacent word coupling should be negligible. However, digit line coupling along the easy axis should be more pronounced.

As noted by Figures 28 and 31 adequate margins can be obtained. These results correspond to the low density configuration (word lines on 8 mil centers, sense lines on 12 mil centers) of the one and two locations per bit devices respectively.

Figure 29 shows the disturb margins for a high density device (word lines on 4 mil centers, sense lines on 8 mil centers). It can be seen that for the unipolar disturbs the margins are inadequate. The bipolar disturb did improve margins, but they are less desirable than the ones demonstrated by Figure 28 for the lower density.

In order to demonstrate that the digit line spacing is the dominant factor, a test was performed on a mixed density. For this test the digit line spacing was increased back to 12 mil centers with the word lines remaining on 4 mil centers.

The disturb characteristics are shown in Figure 30. The increase in margins and the effect of the bipolar disturb are clearly demonstrated.

Since a high density area for the two locations per bit was not available, only the low density area was tested. Figure 31 shows that the signal will almost double as expected. Margins remain about the same as the single location per bit device, however, the effect of the bipolar disturb is more pronounced.

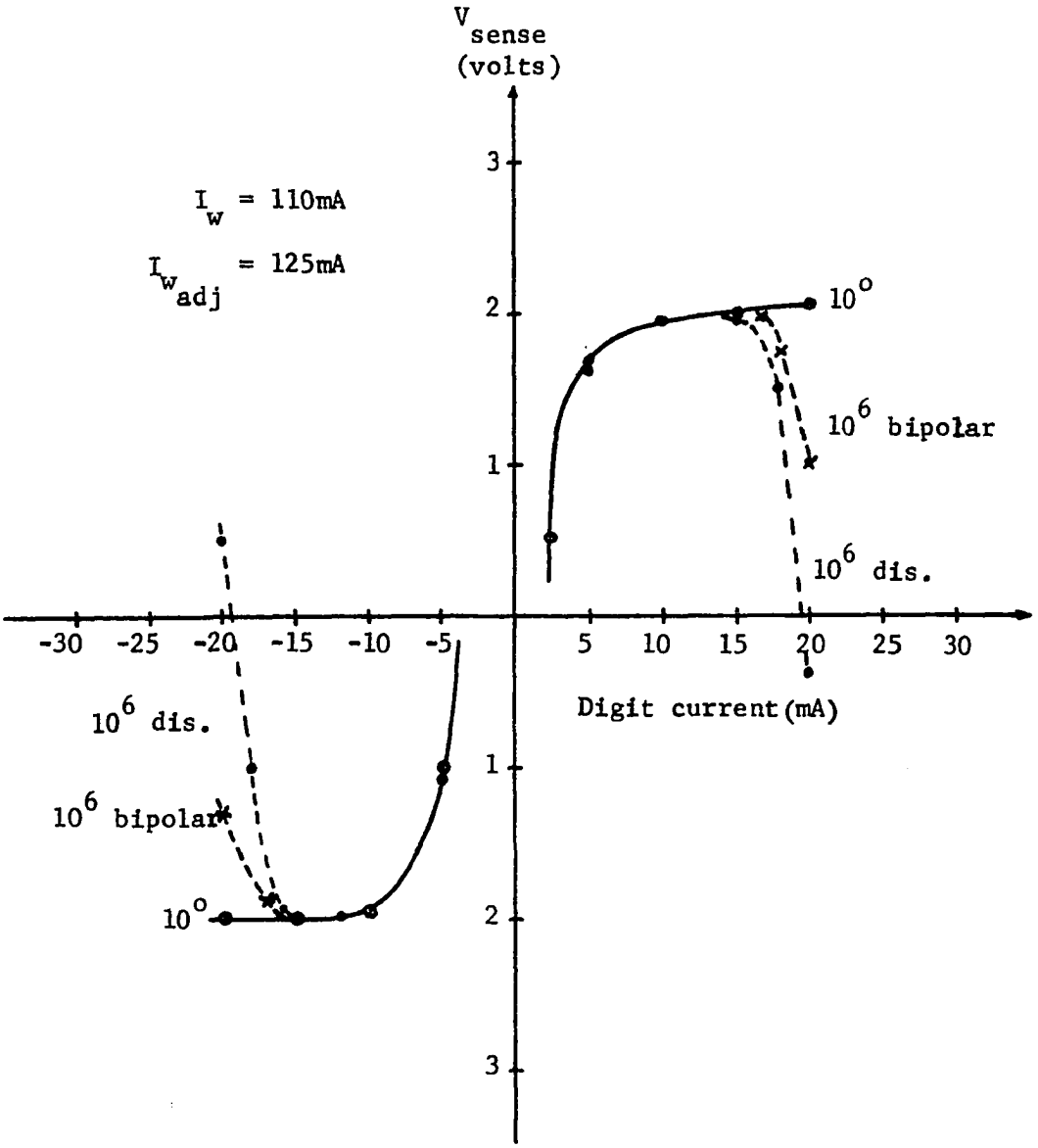


Figure 28. Disturb characteristics of the low density, single location per bit area

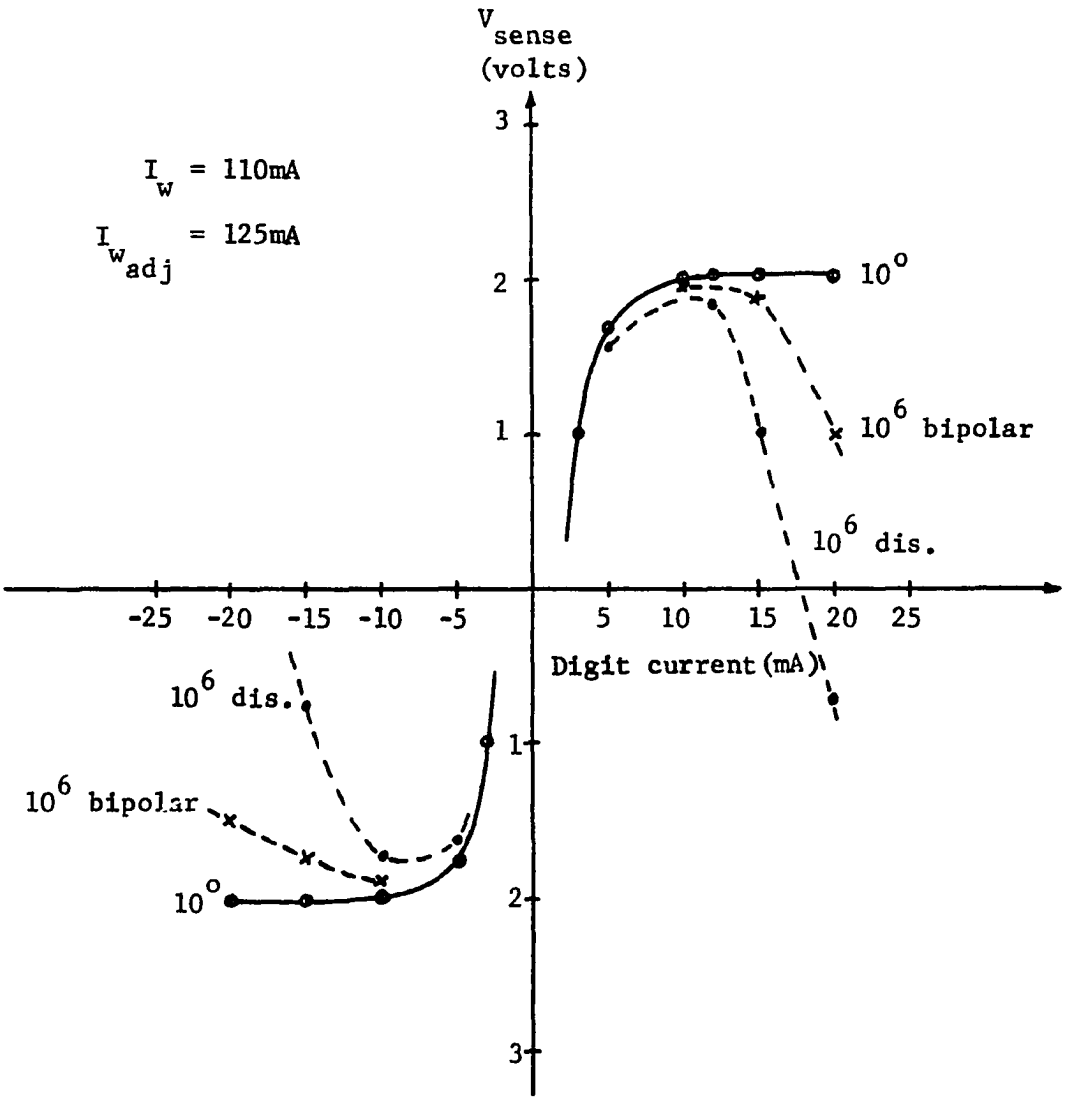


Figure 29. Disturb characteristics of the high density, single location per bit area

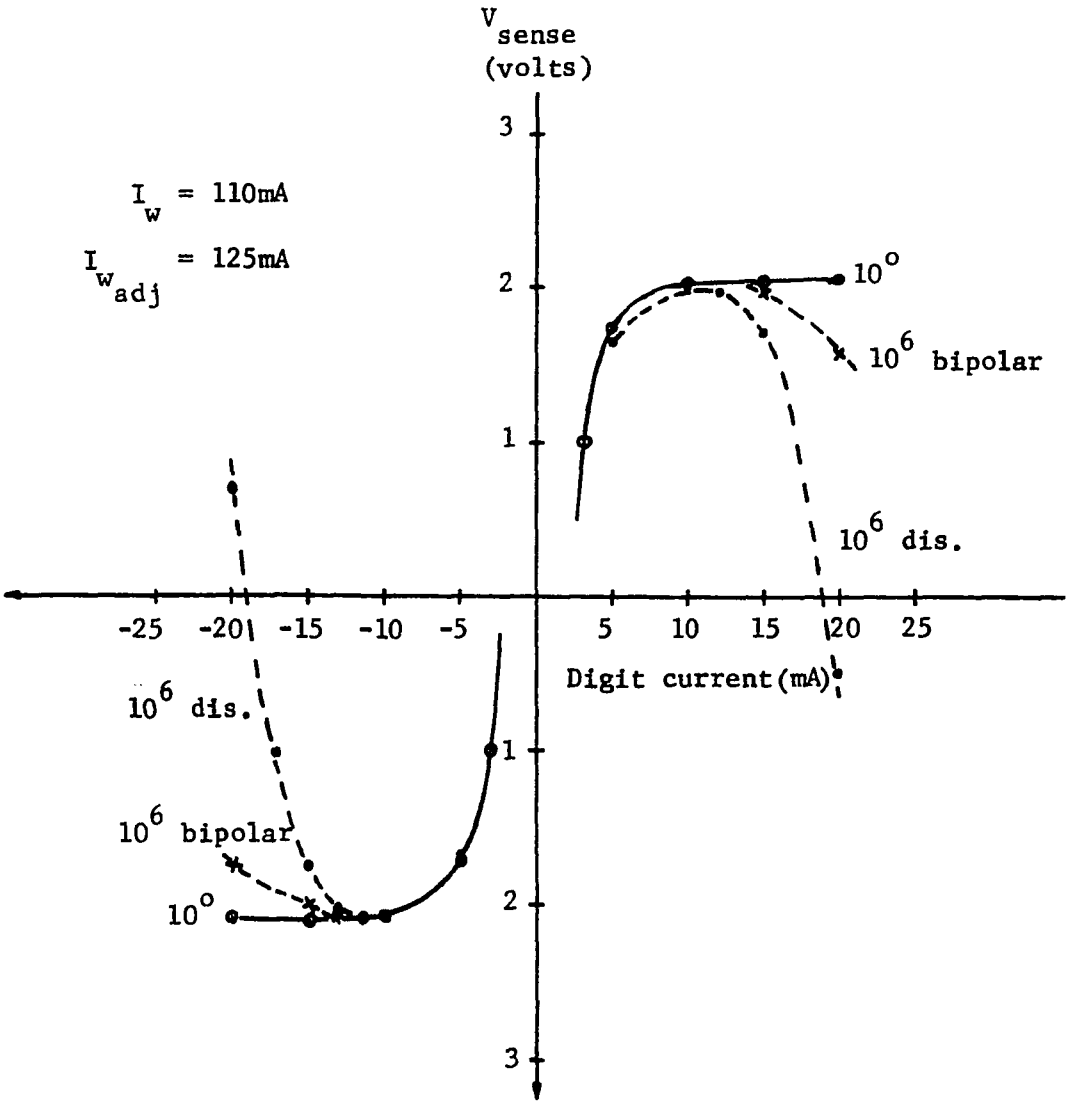


Figure 30. Disturb characteristics of mixed density, single location per bit area. Word lines on 4 mil centers sense lines on 12 mil centers

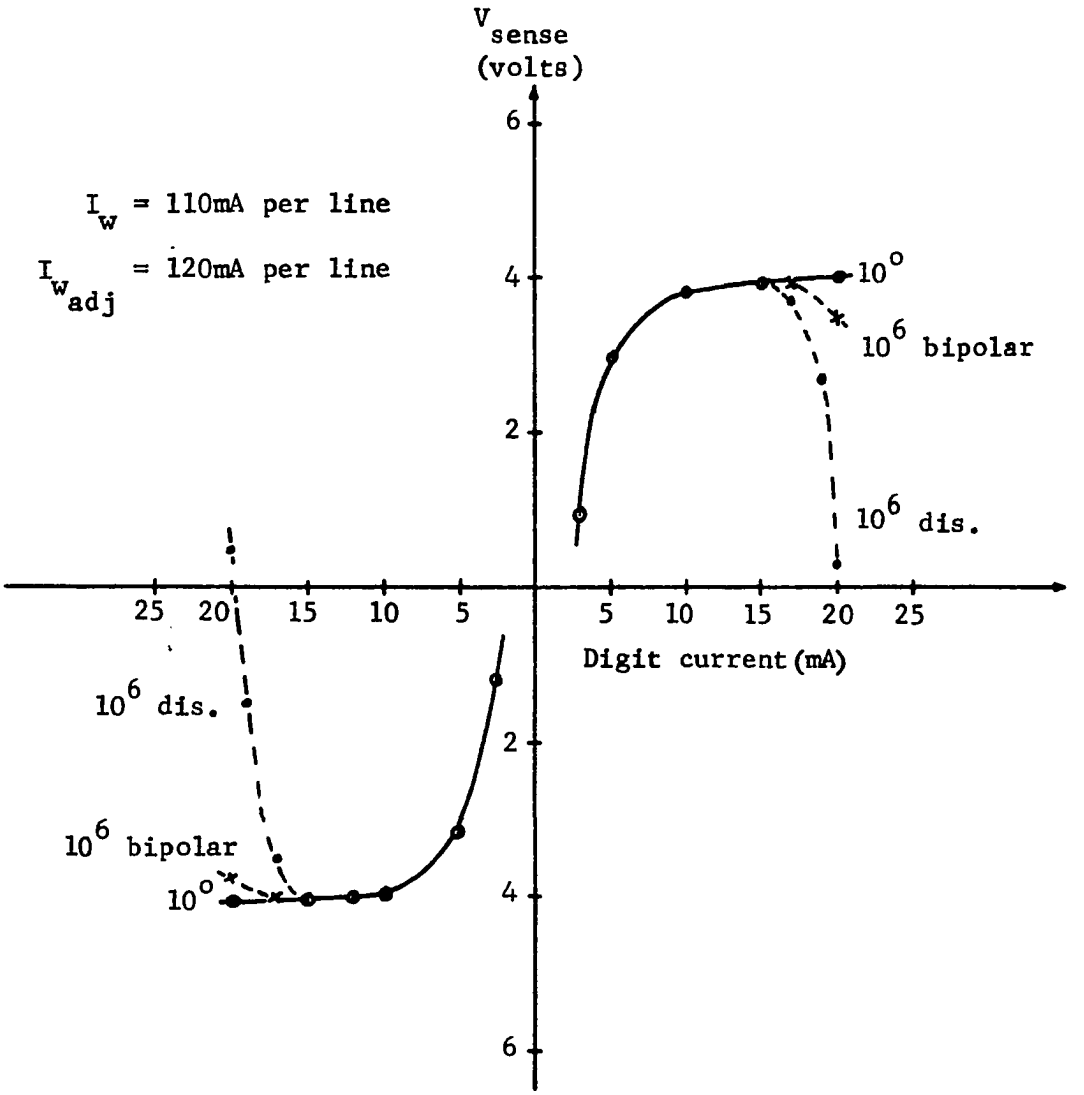


Figure 31. Disturb characteristics of the low density, two locations per bit area

X. DISCUSSION AND CONCLUSION

The feasibility of building a DRO magnetic thin film memory with a capacity of 10 million bits and high data rate has been demonstrated.

It should not be unreasonable to expect that a fully populated memory will operate with less than 1.0 μsec cycle time. Although the partially populated memory achieved a cycle time of less than 500 nsec, it should be remembered that sacrifices will have to be made when all peripheral electronics and all modules are assembled. For a 1024 digit lines, the 1024 Megabits/sec data rate makes this memory more than adequate to operate as a main memory or a back up store to any high-speed main memory.

Sense signals of 1.5 to 2.5 mV are large enough for standard detection. However, special attention ought to be given to the development of simple sense amplifiers with adequate signal to noise ratio and good digit transient recovery with long digit lines.

Power requirements for a memory of this size are considerable. The cost of high data rates is most pronounced by the sense-digit power requirements. Most of the power consumption is attributed to these circuits. From the partially populated memory it is estimated that the power requirements of the sense-digit amplifiers and related TTL logic is about 170 amps at +5 volts and 75 amps at -5 volts. (A more conservative design can easily cut this requirements by a factor of 4.) The total power requirements of the fully populated memory is estimated at about 1500 watts. It is assumed that if integrated circuits are designed, this can be lowered substantially.

Based on the short cost estimate presented previously, it would be reasonable to assume a cost of about 0.25 cents per bit for the fully populated memory. However, it would be difficult to predict the cost of such a device.

It should be mentioned that on the average the number of connections for this memory will be less than a comparable LSI memory. In addition, dimensional control of magnetic cells is not as stringent as for LSI memory devices. These advantages can be translated directly into cost reduction.

Good batch fabrication processes should lead to low cost given reasonable large production. However, a rather large economic commitment is needed in order to realize the full potential of such a device. Customized low cost IC peripheral electronics as suggested in this thesis is designed to achieve minimum cost via optimized packages. The lack of immediate availability of such IC packages reflects upon the initial economic commitment.

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